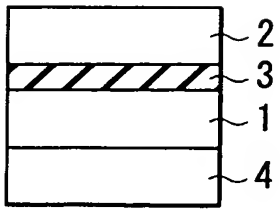
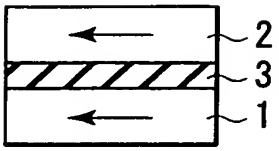
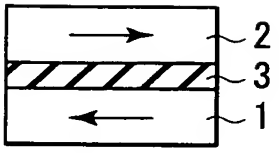


FIG. 1



PARALLEL
(SMALLER RESISTANCE)

FIG. 2A



ANTI-PARALLEL
(LARGER RESISTANCE)

FIG. 2B

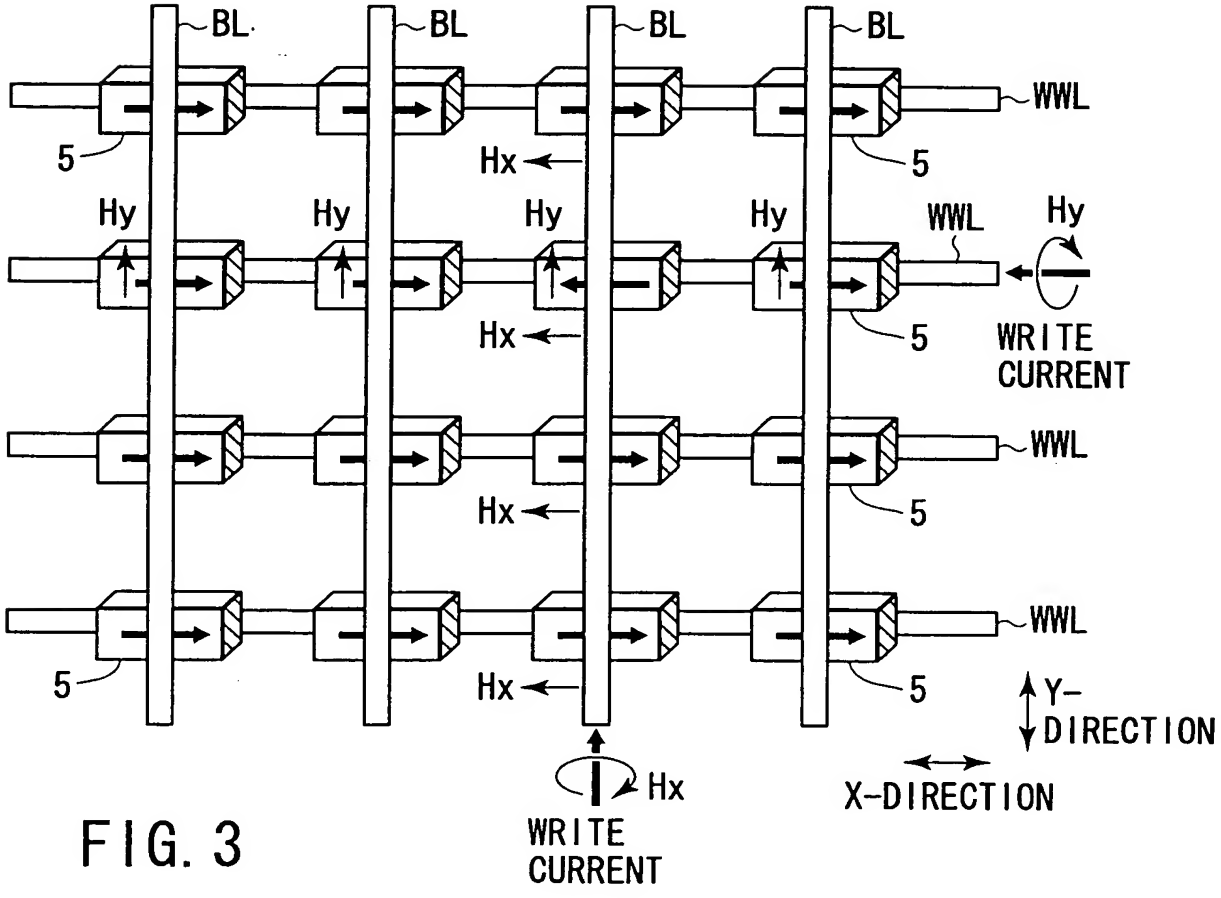


FIG. 3

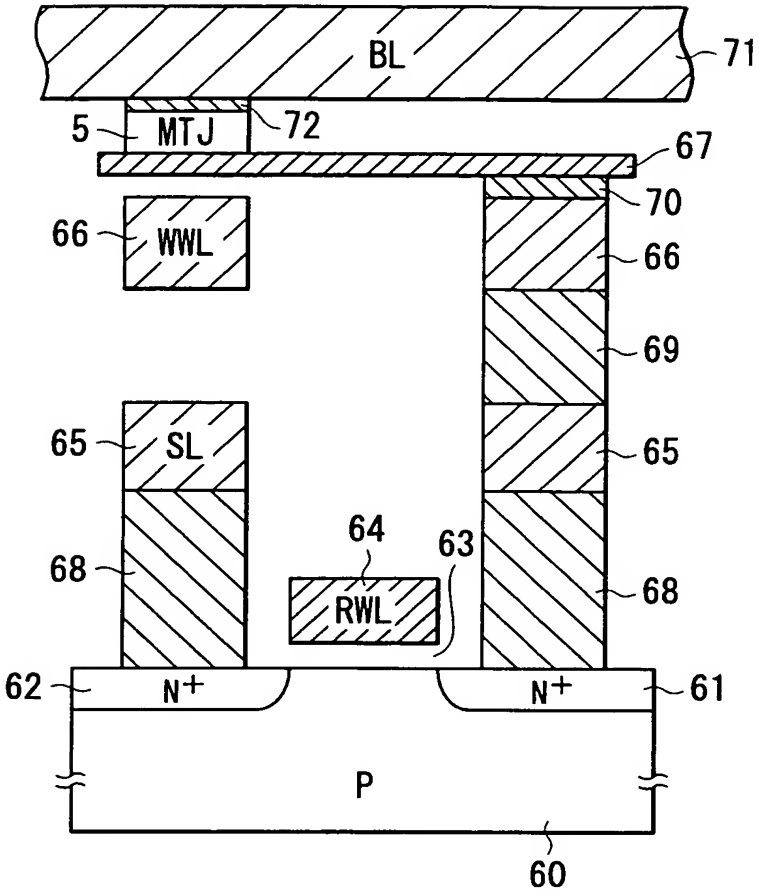

BL
71
5
MTJ
72
67
70
66
WWL
66
69
65
SL
65
64
63
68
RWL
68
62
N+
N+
61
P
60

FIG. 4

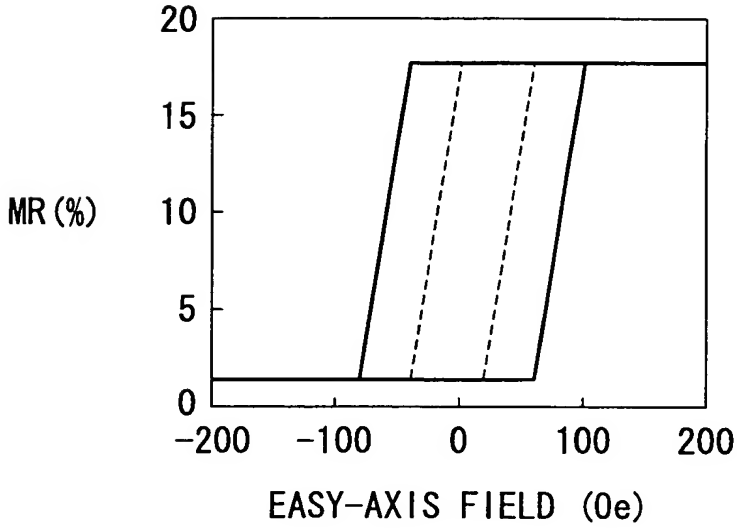

20
15
MR (%)
10
5
0
-200
-100
0
100
200
EASY-AXIS FIELD (Oe)

FIG. 5

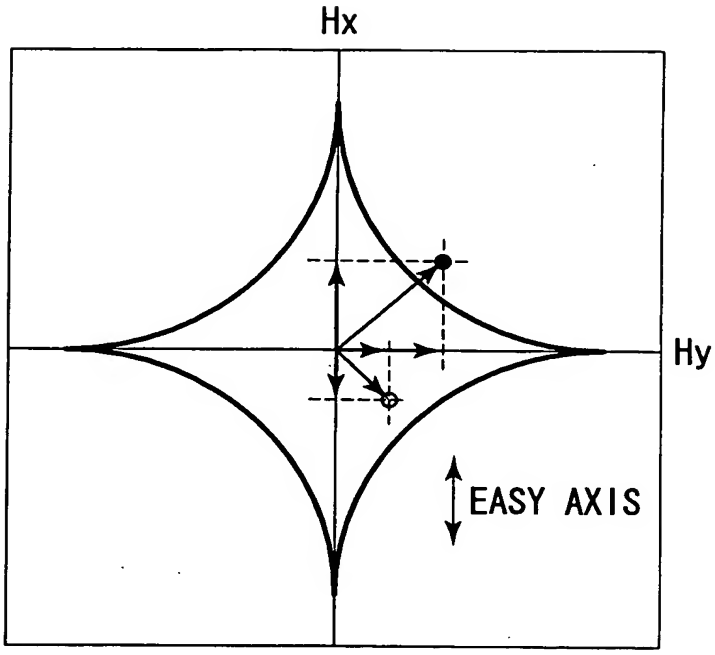


FIG. 6

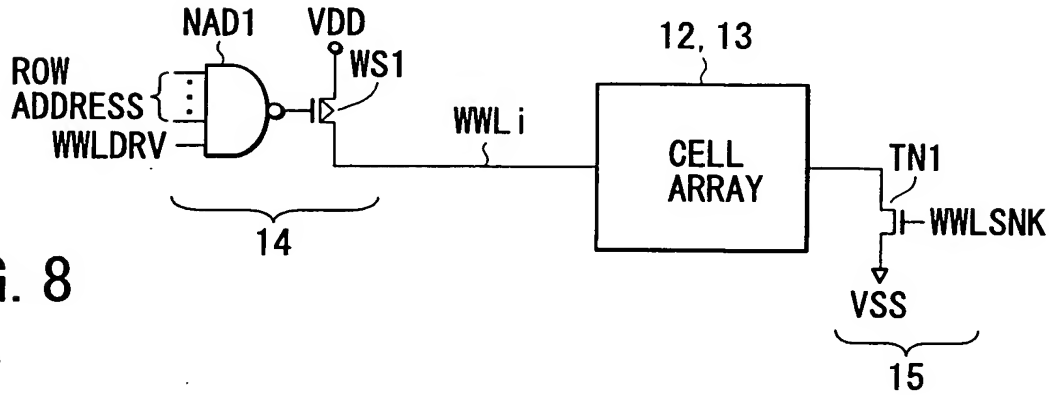


FIG. 8

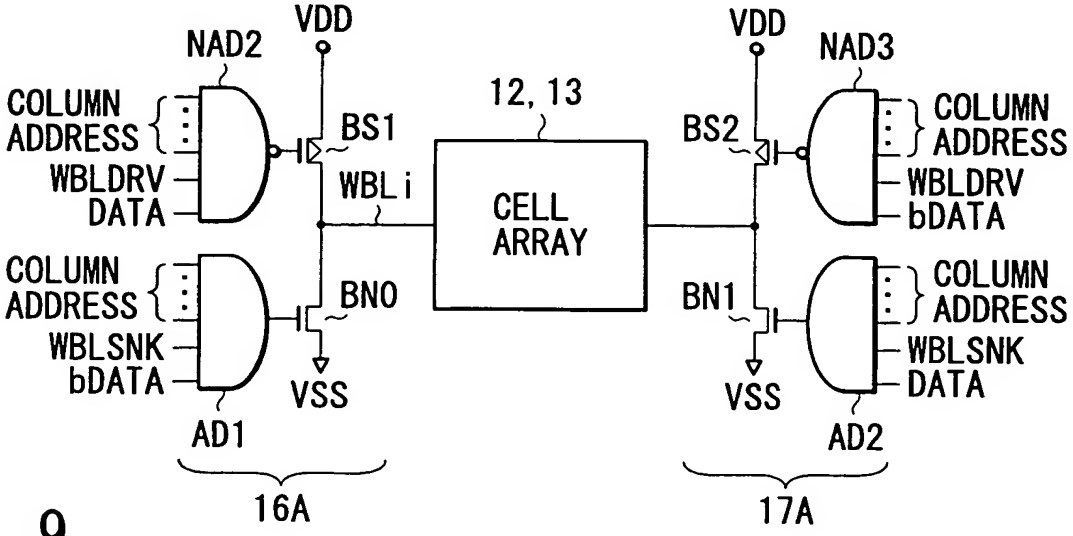


FIG. 9

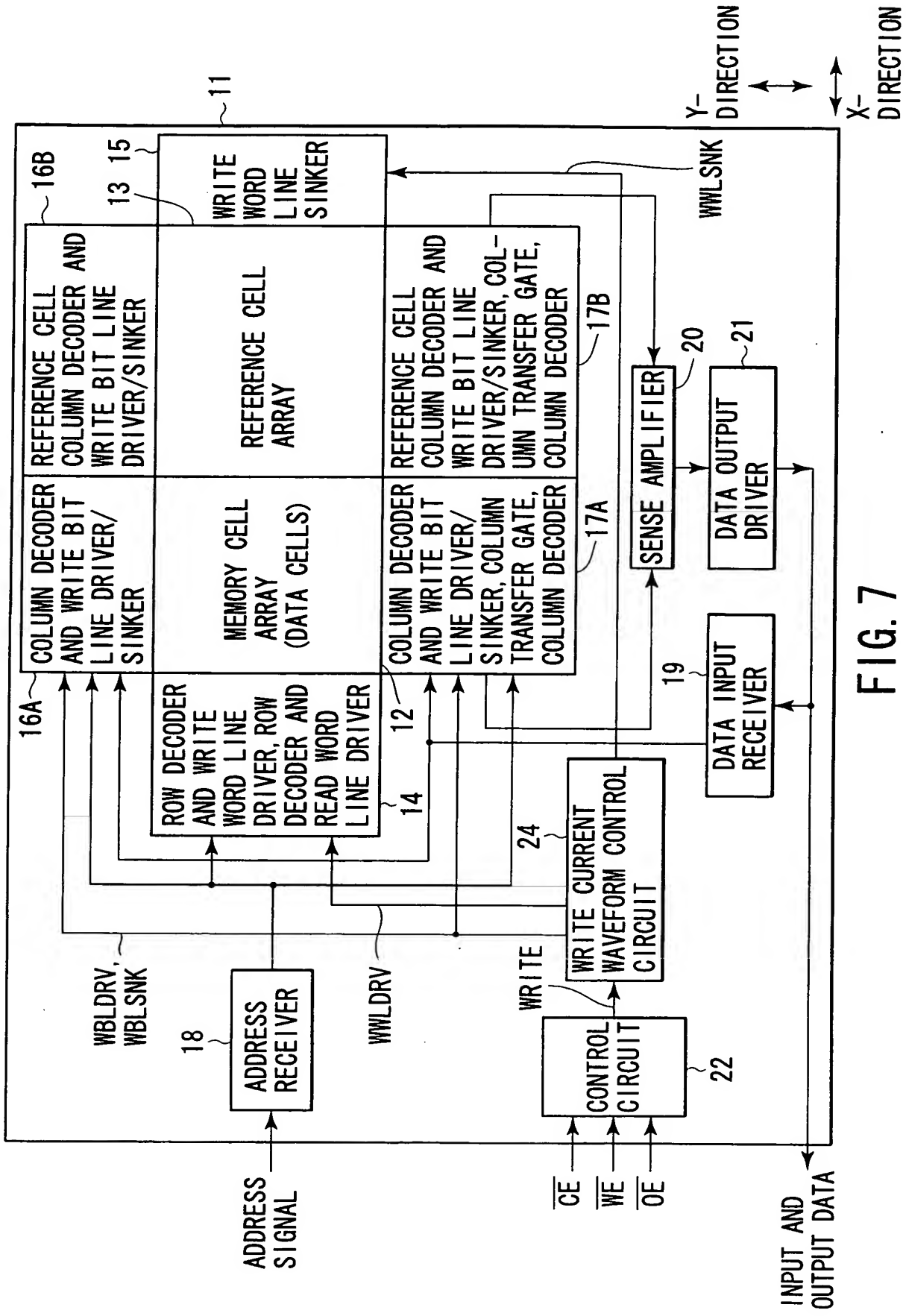

11
Y-DIRECTION
X-DIRECTION
16B
13 15
WRITE WORD LINE SINKER
WWLSNK
REFERENCE CELL COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER
REFERENCE CELL ARRAY
REFERENCE CELL COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER, COLUMN TRANSFER GATE, COLUMN DECODER
17B
20
21
SENSE AMPLIFIER
DATA OUTPUT DRIVER
COLUMN DECODER AND WRITE BIT LINE DRIVER/ SINKER
MEMORY CELL ARRAY (DATA CELLS)
COLUMN DECODER AND WRITE BIT LINE DRIVER/ SINKER, COLUMN TRANSFER GATE, COLUMN DECODER
17A
16A
ROW DECODER AND WRITE WORD LINE DRIVER, ROW DECODER AND READ WORD LINE DRIVER
12
14
19
DATA INPUT RECEIVER
24
WRITE CURRENT WAVEFORM CONTROL CIRCUIT
WBLDRV, WBLSNK
18
ADDRESS RECEIVER
WWLDRV
WRITE
CONTROL CIRCUIT
22
ADDRESS SIGNAL
CE
WE
OE
INPUT AND OUTPUT DATA

FIG. 7

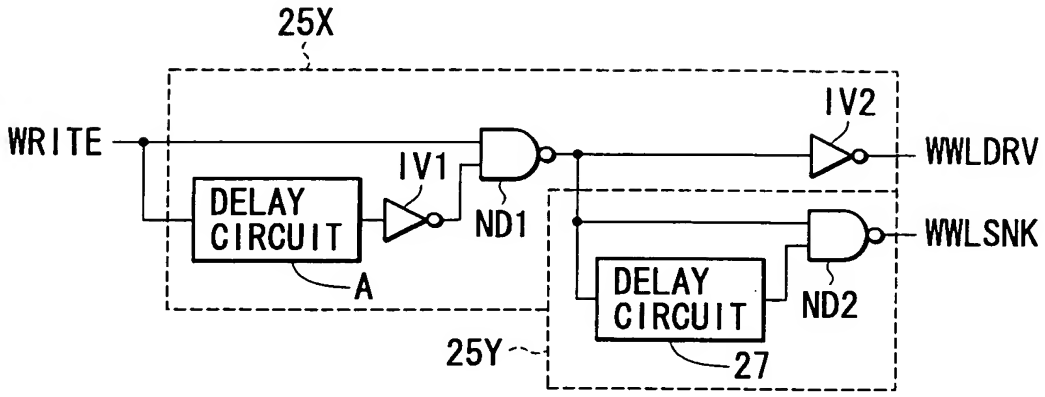


FIG. 10

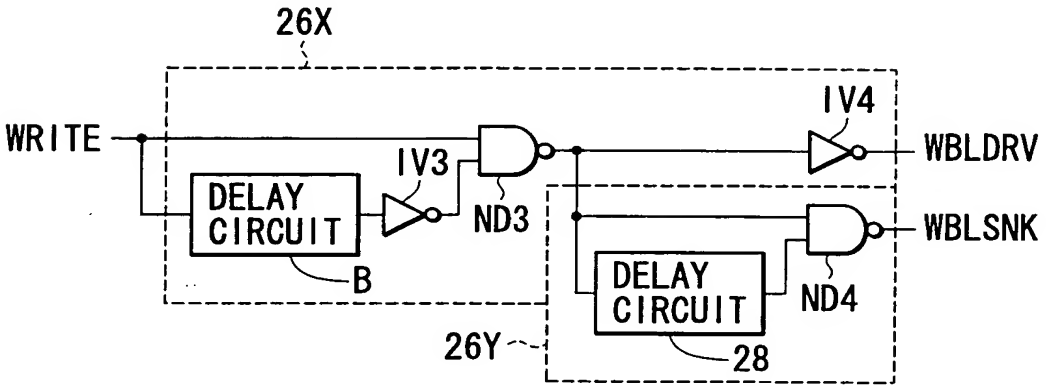


FIG. 11

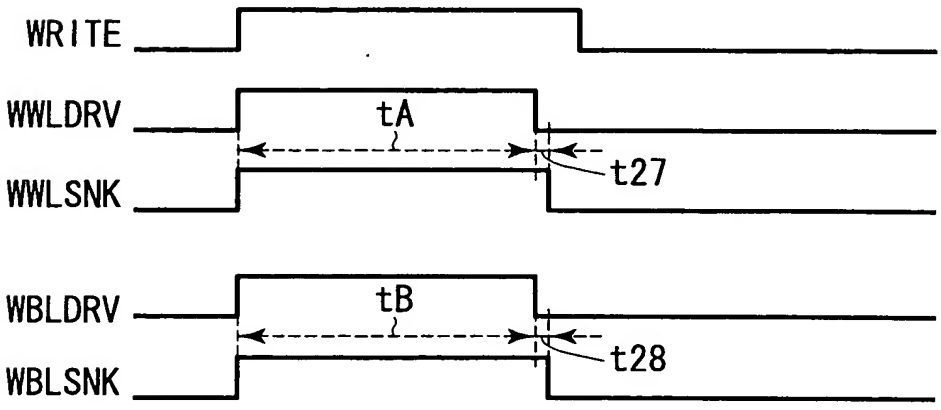


FIG. 12

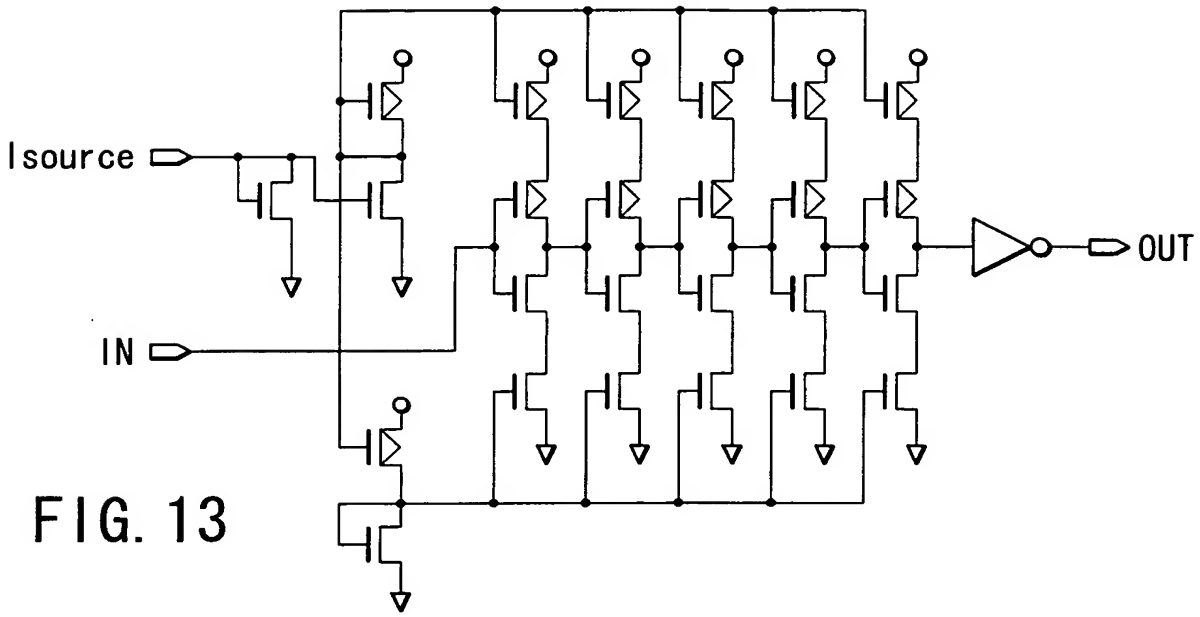


FIG. 13

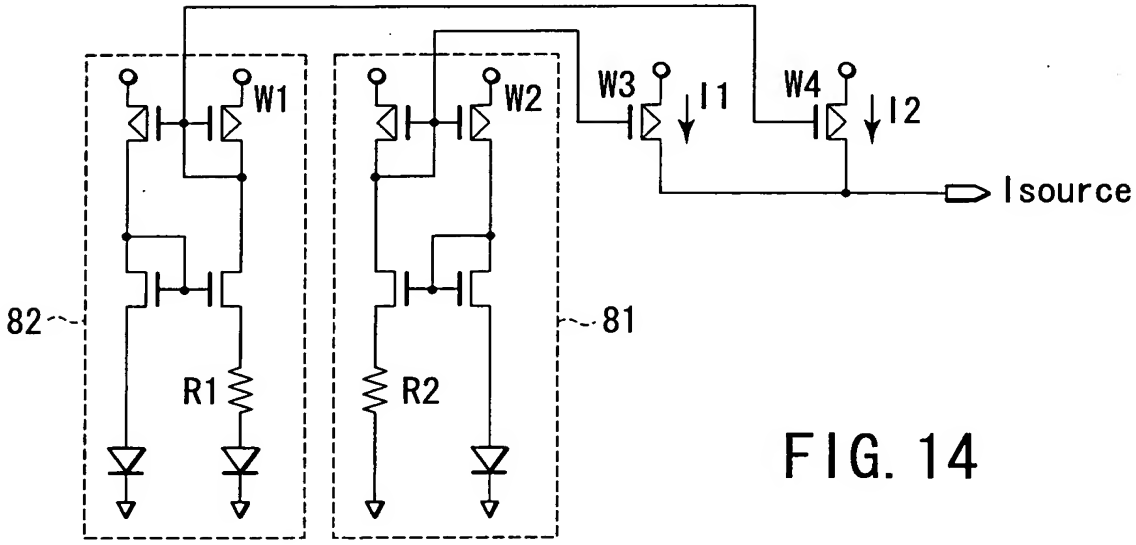


FIG. 14

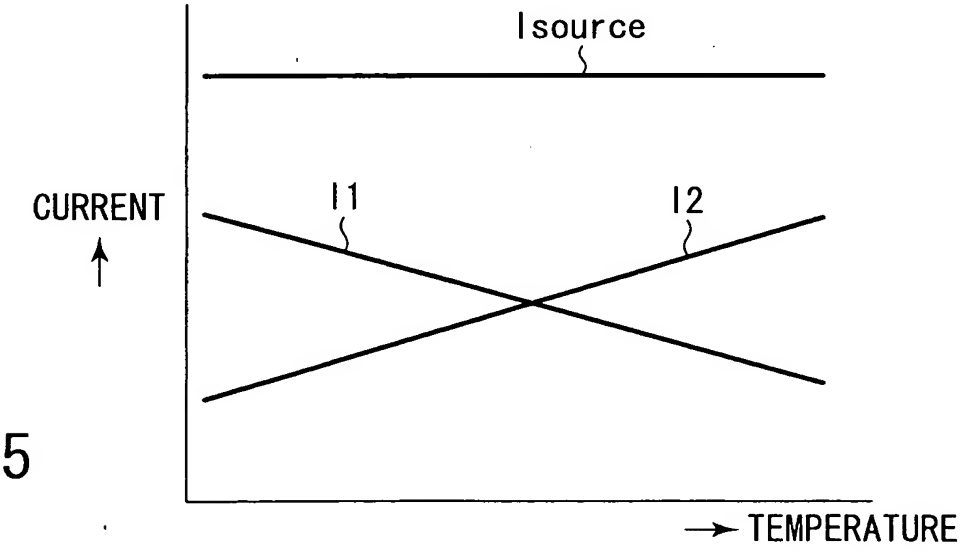


FIG. 15

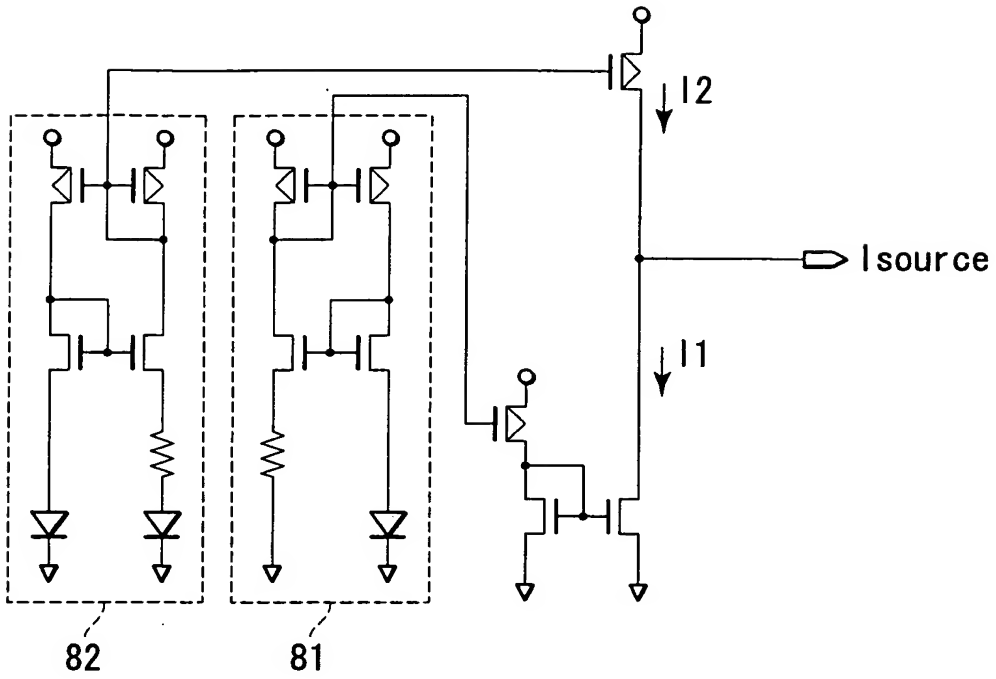


FIG. 16

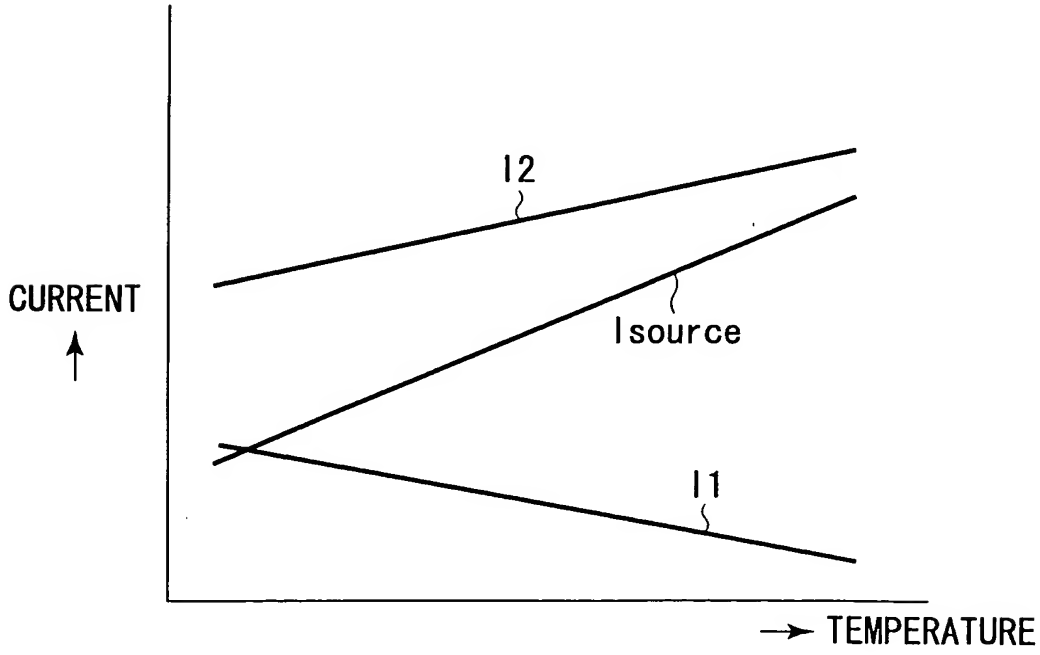


FIG. 17

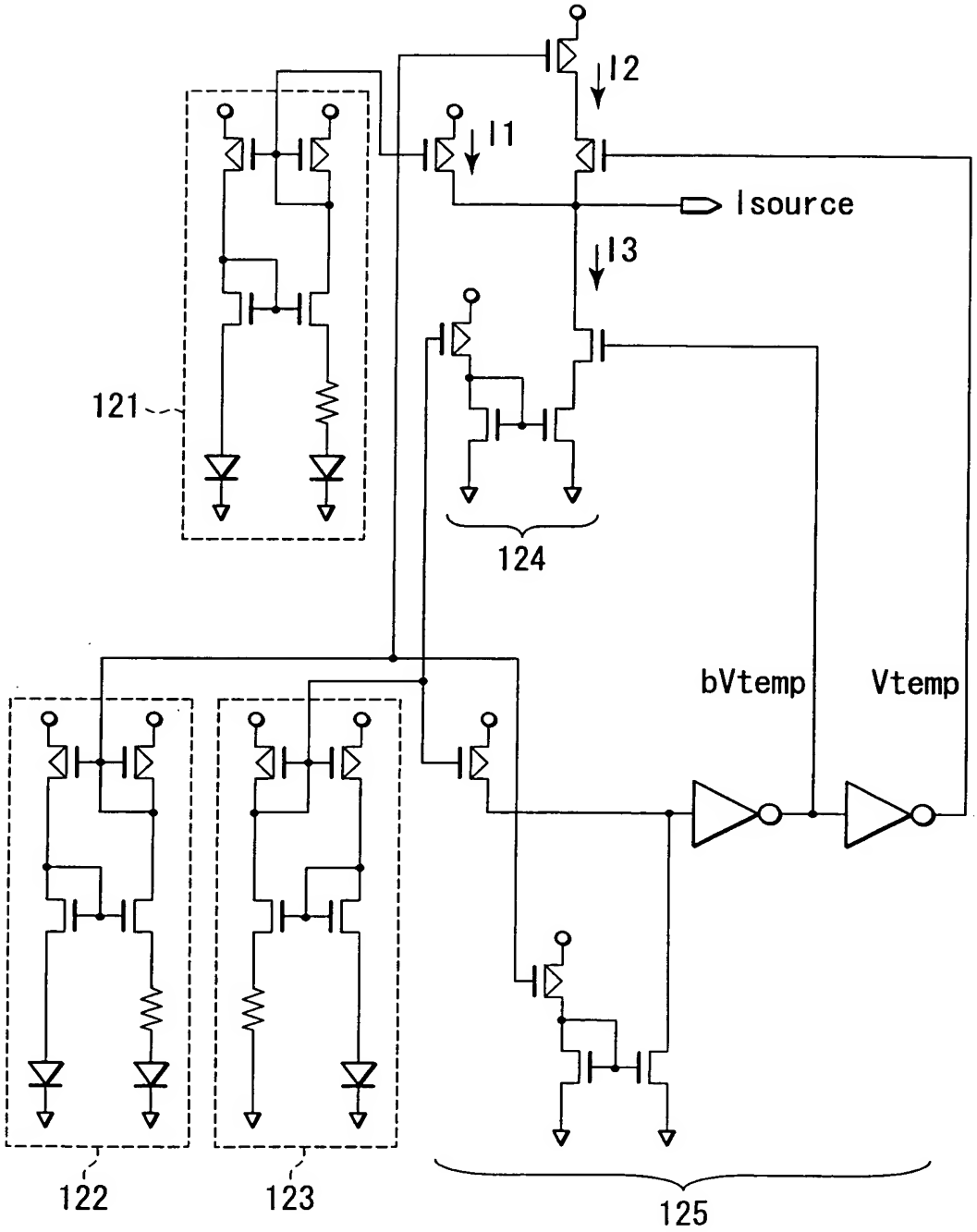


FIG. 18

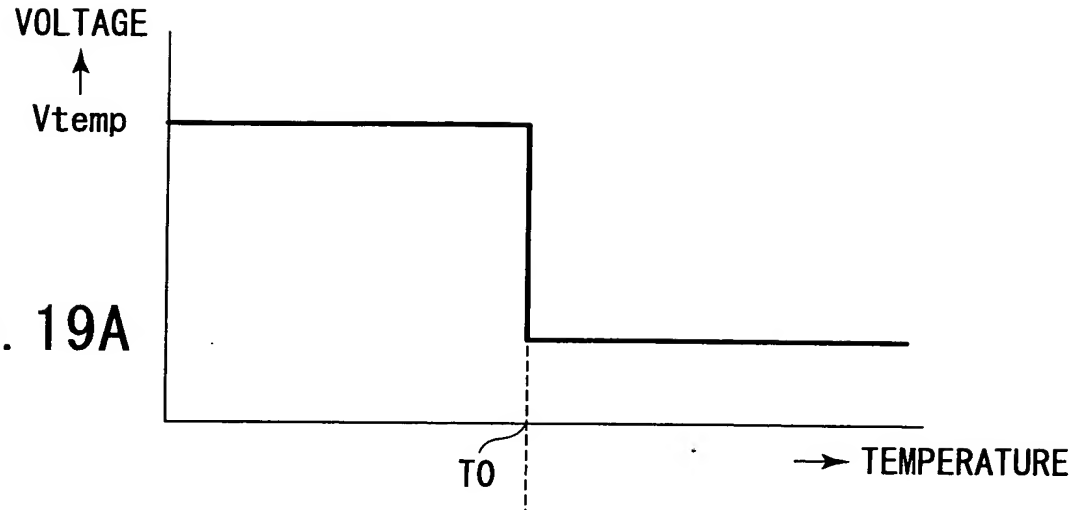


FIG. 19A

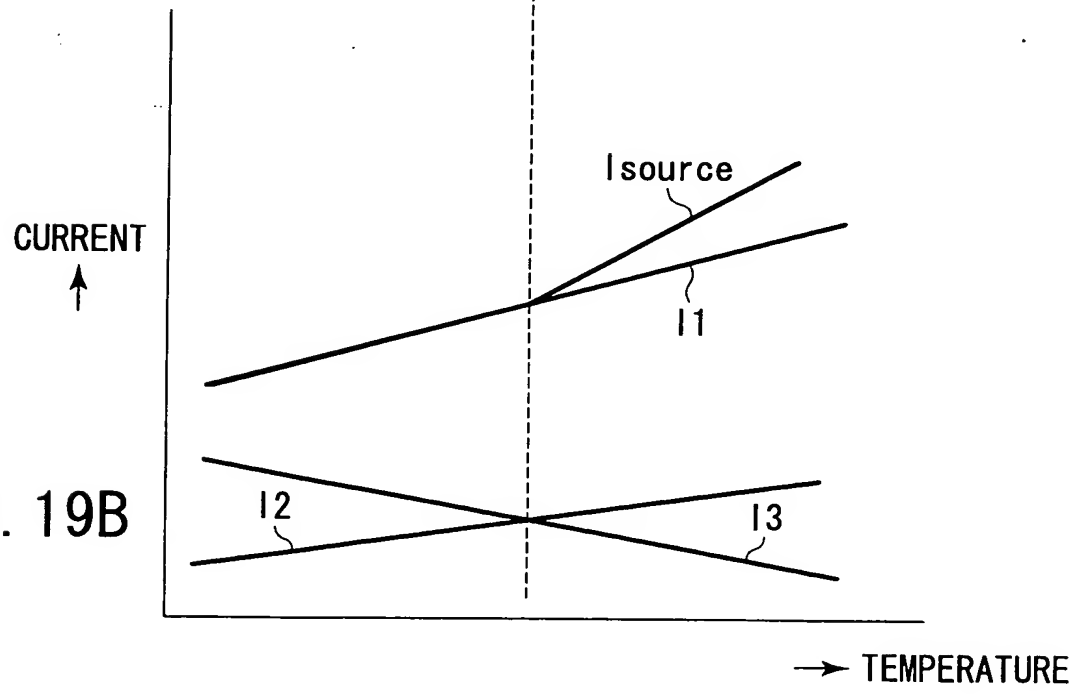


FIG. 19B

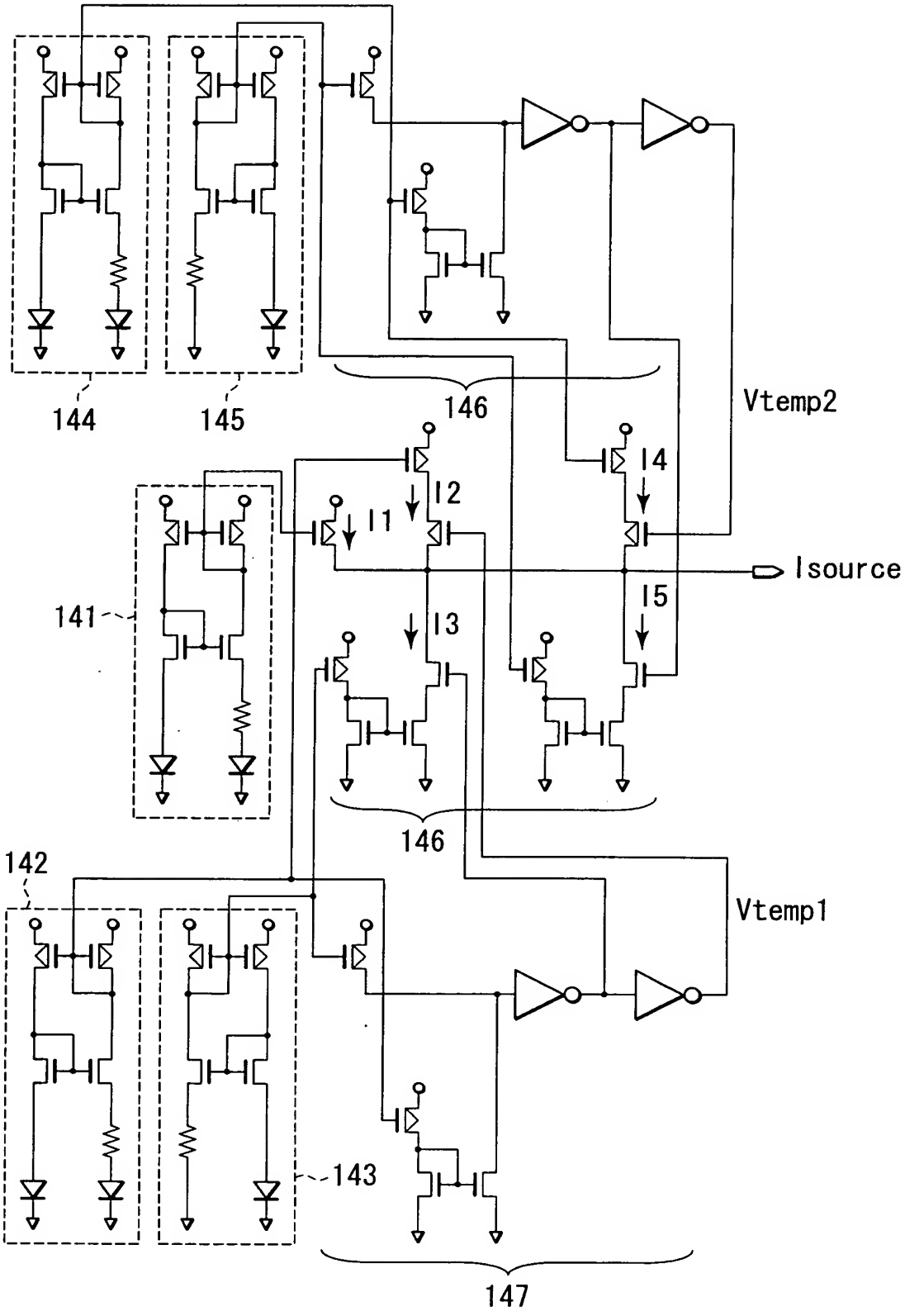

144
145
146
Vtemp2
14
12
11
Isource
15
141
13
146
142
Vtemp1
143
147

FIG. 20

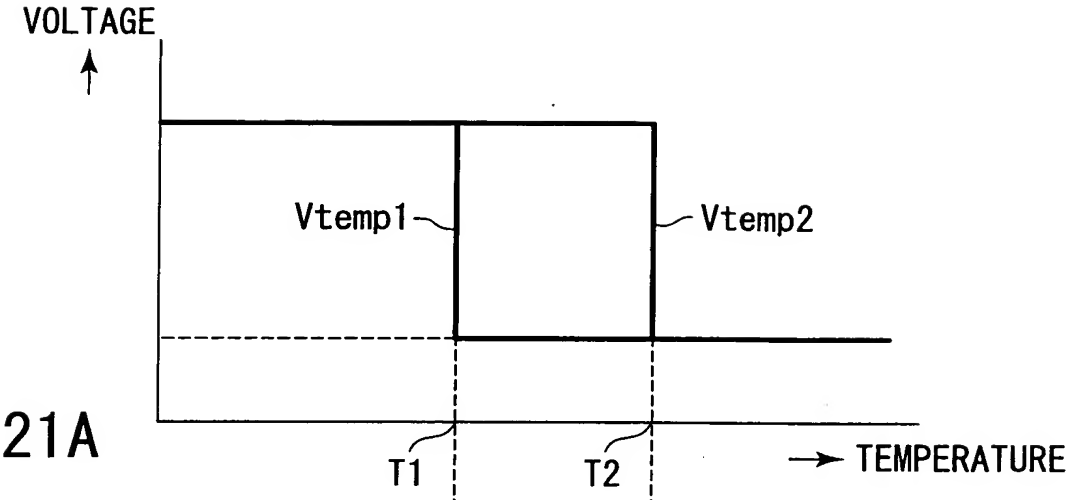


FIG. 21A

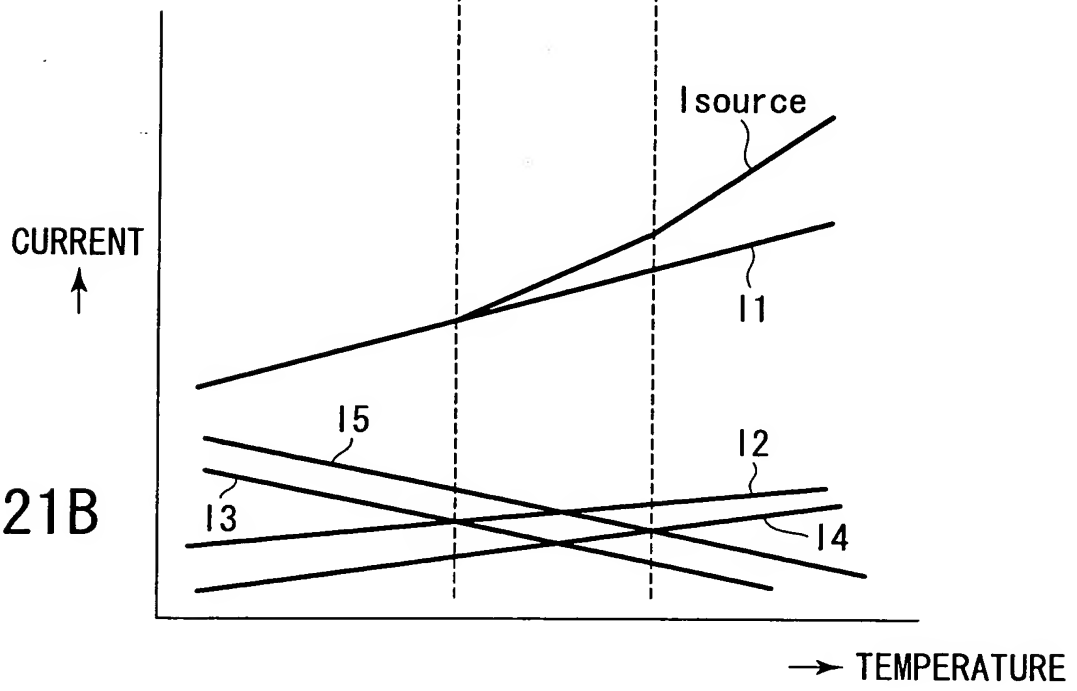


FIG. 21B

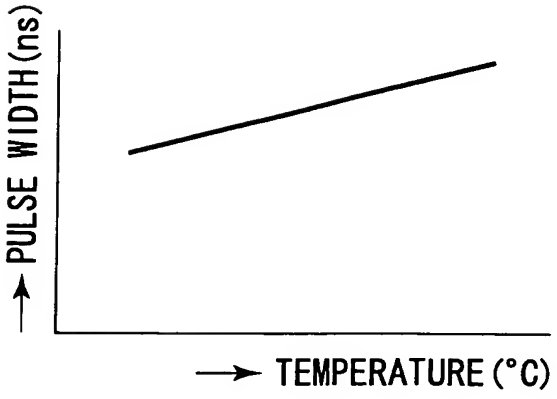


FIG. 22

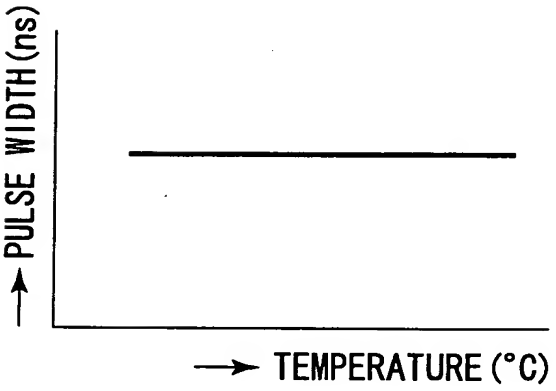


FIG. 23

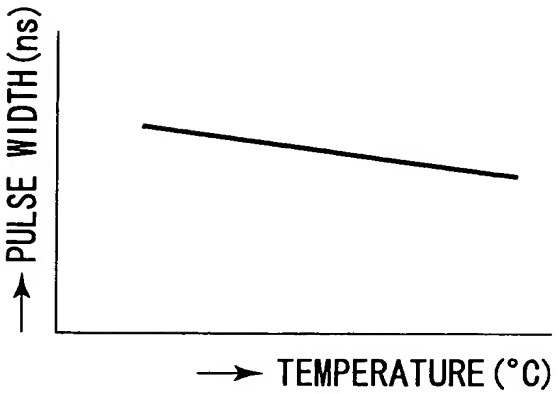


FIG. 24

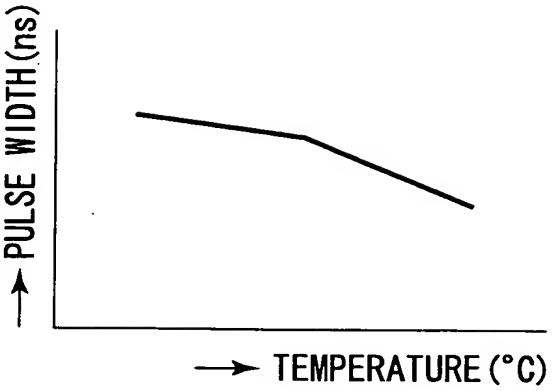


FIG. 25

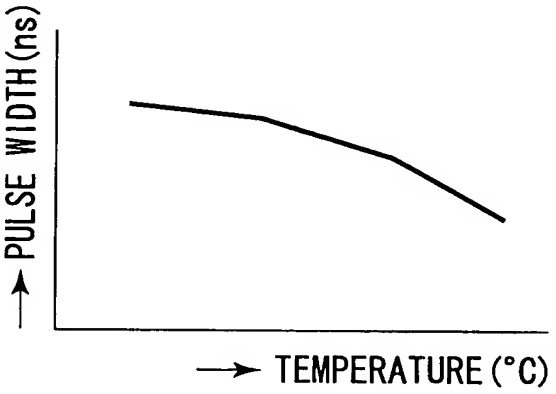


FIG. 26

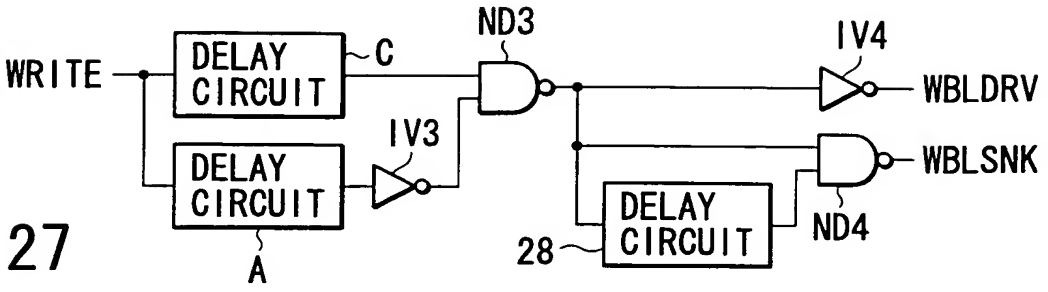


FIG. 27

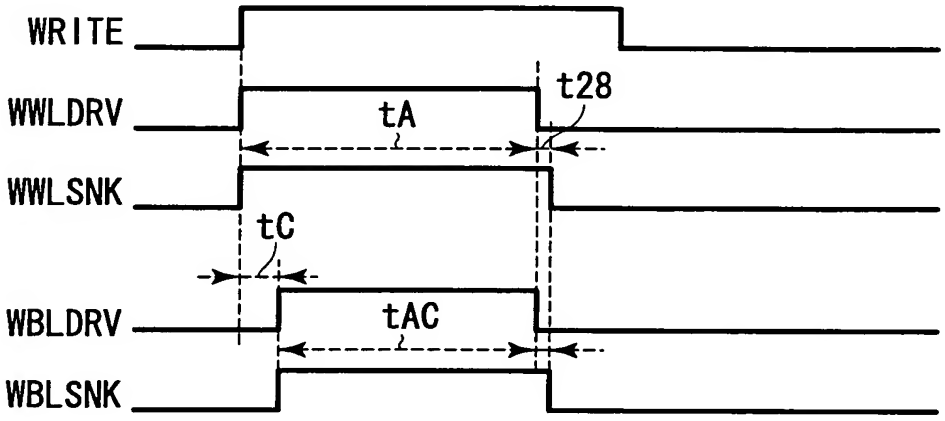


FIG. 28

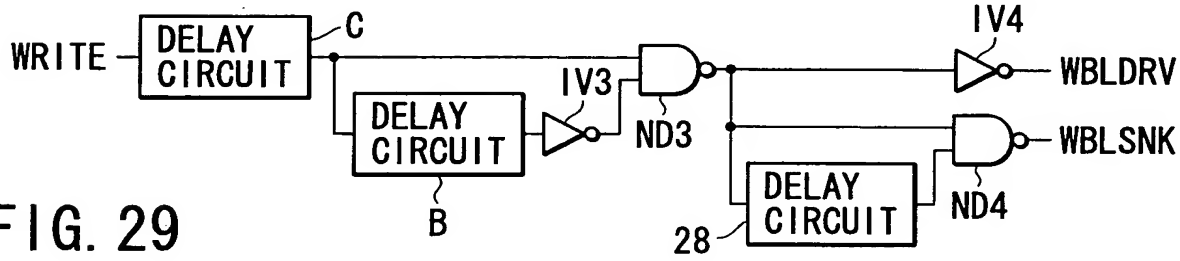


FIG. 29

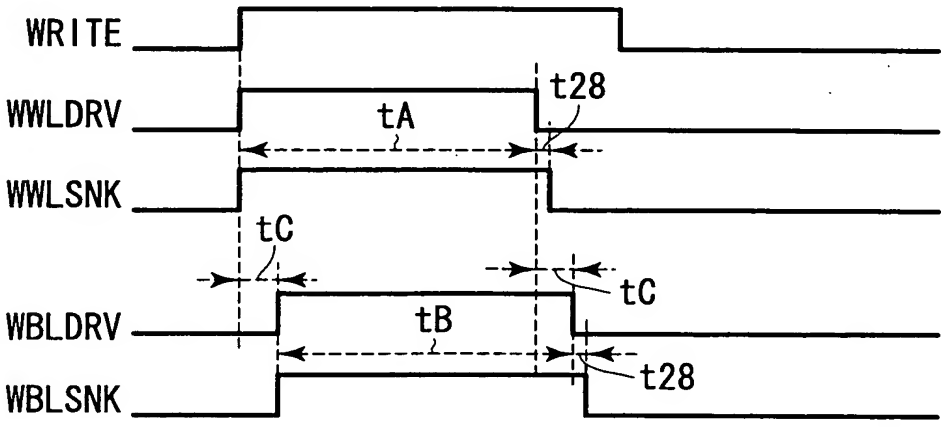


FIG. 30

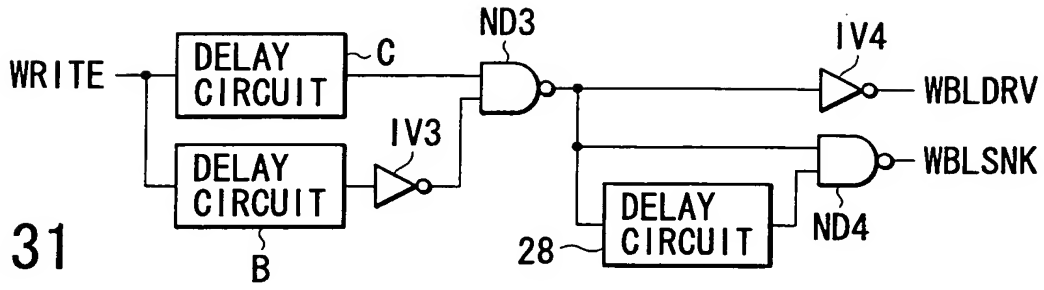


FIG. 31

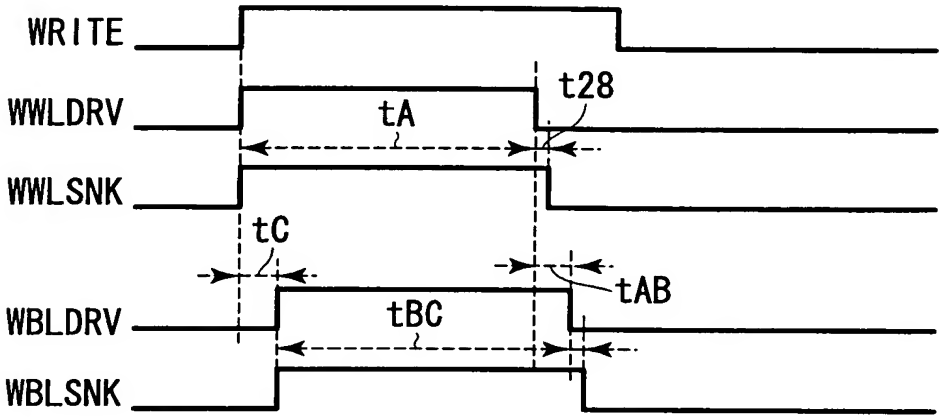


FIG. 32

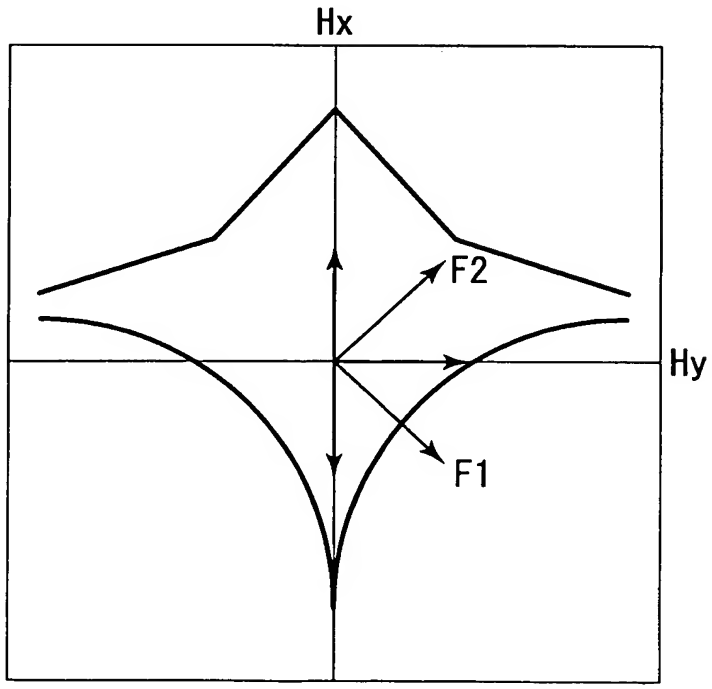


FIG. 33

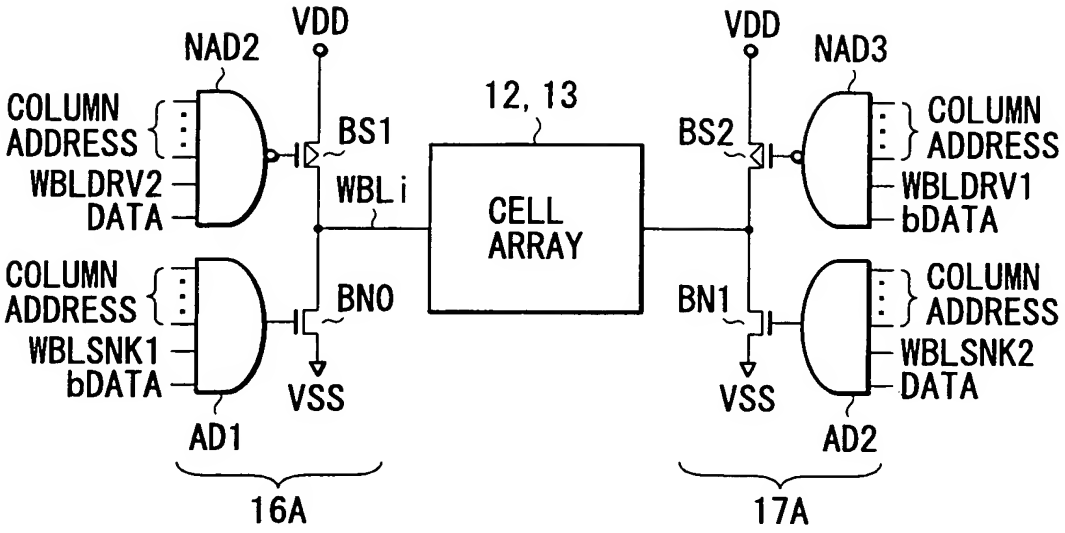


FIG. 34

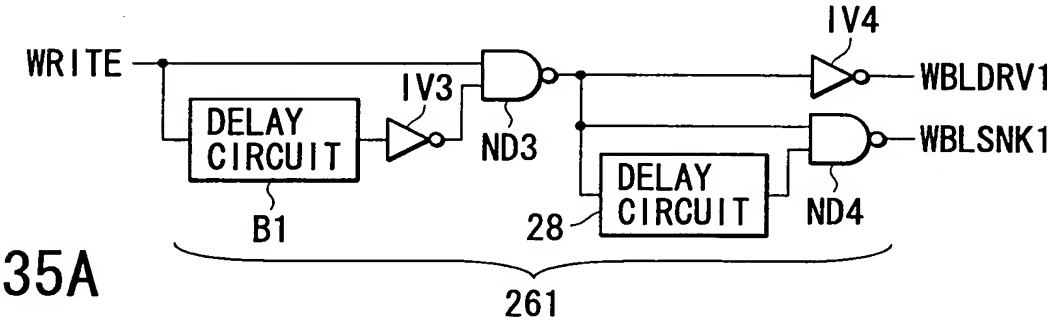


FIG. 35A

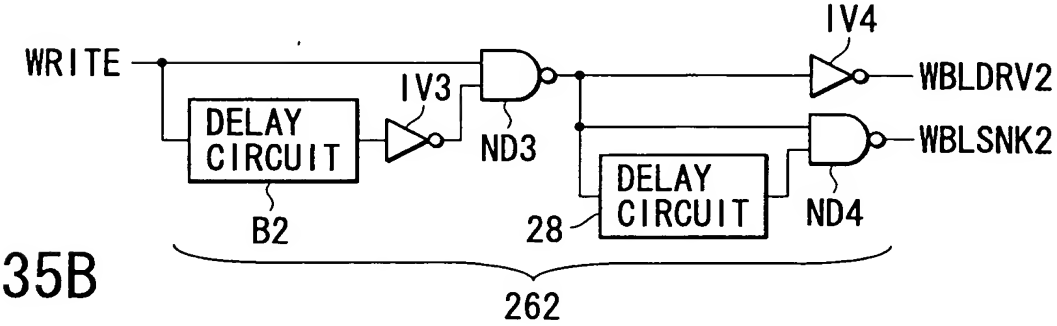


FIG. 35B

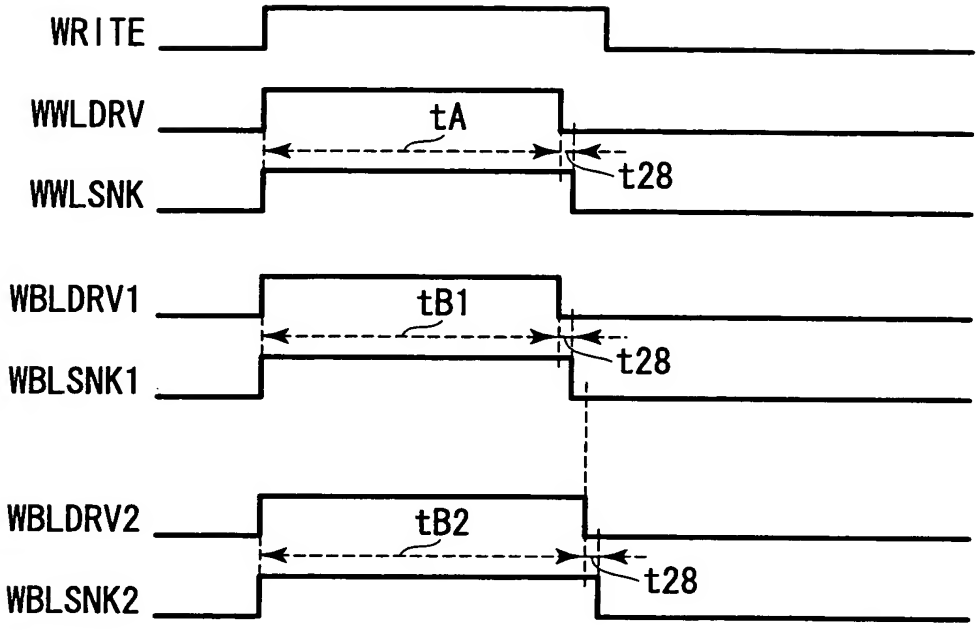

WRITE
WWLDRV
tA
t28
WWLSNK
WBLDRV1
tB1
t28
WBLSNK1
WBLDRV2
tB2
t28
WBLSNK2

FIG. 36

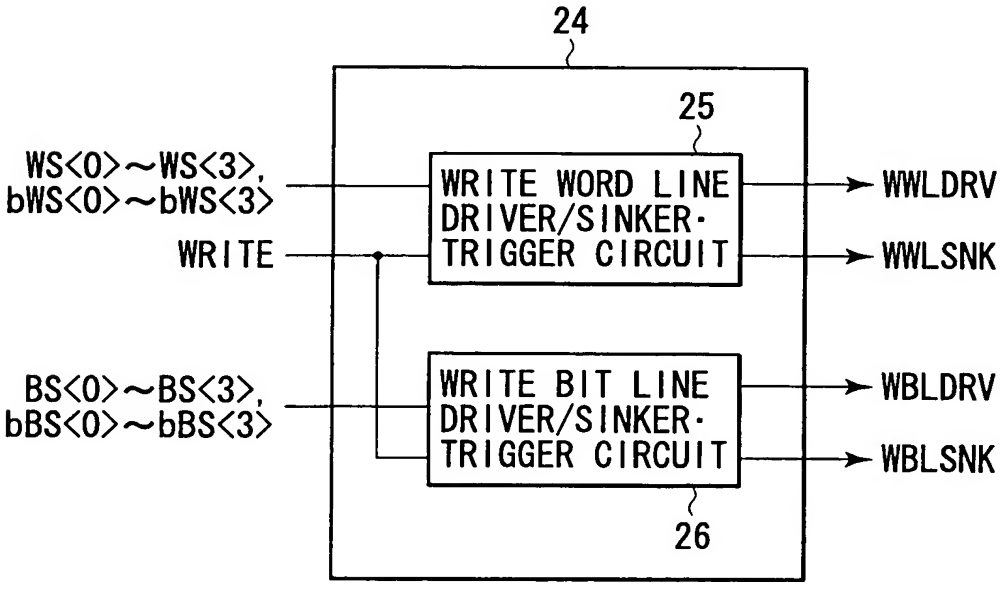

24
25
WS<0>~WS<3>,
bWS<0>~bWS<3>
WRITE
WRITE WORD LINE
DRIVER/SINKER·
TRIGGER CIRCUIT
WWLDRV
WWLSNK
BS<0>~BS<3>,
bBS<0>~bBS<3>
WRITE BIT LINE
DRIVER/SINKER·
TRIGGER CIRCUIT
WBLDRV
WBLSNK
26

FIG. 38

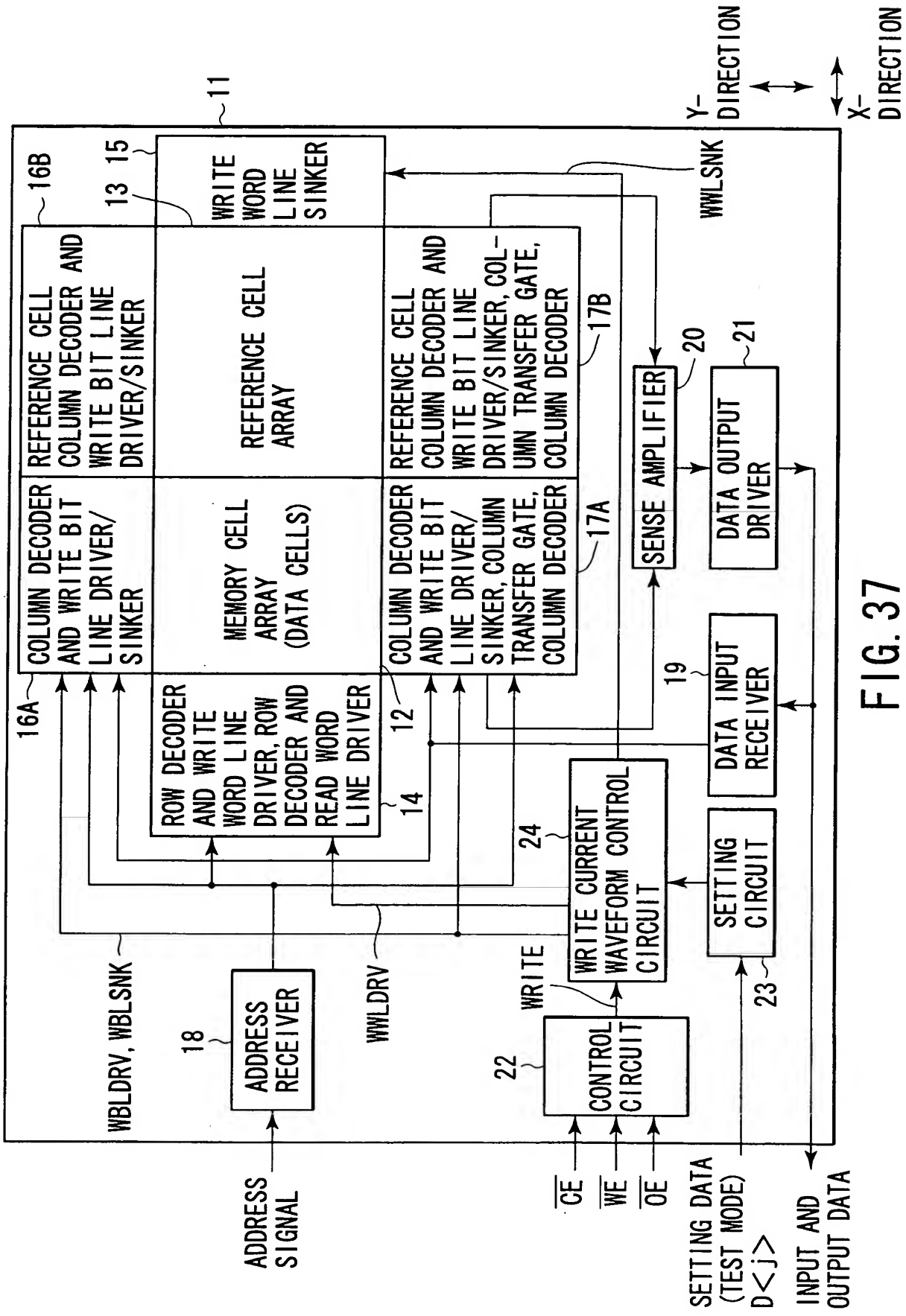

11
Y-DIRECTION
X-DIRECTION
16B
13
15
WRITE WORD LINE SINKER
WWLSNK
REFERENCE CELL COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER
REFERENCE CELL ARRAY
REFERENCE CELL COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER, COLUMN TRANSFER GATE, COLUMN DECODER
17B
20
21
SENSE AMPLIFIER
DATA OUTPUT DRIVER
16A
COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER
MEMORY CELL ARRAY (DATA CELLS)
COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER, COLUMN TRANSFER GATE, COLUMN DECODER
17A
ROW DECODER AND WRITE WORD LINE DRIVER, ROW DECODER AND READ WORD LINE DRIVER
14
12
19
DATA INPUT RECEIVER
24
WRITE CURRENT WAVEFORM CONTROL CIRCUIT
SETTING CIRCUIT
WBLDRV, WBLSNK
18
ADDRESS RECEIVER
WWLDRV
WRITE
22
CONTROL CIRCUIT
23
ADDRESS SIGNAL
CE
WE
OE
SETTING DATA (TEST MODE) D<j>
INPUT AND OUTPUT DATA

FIG. 37

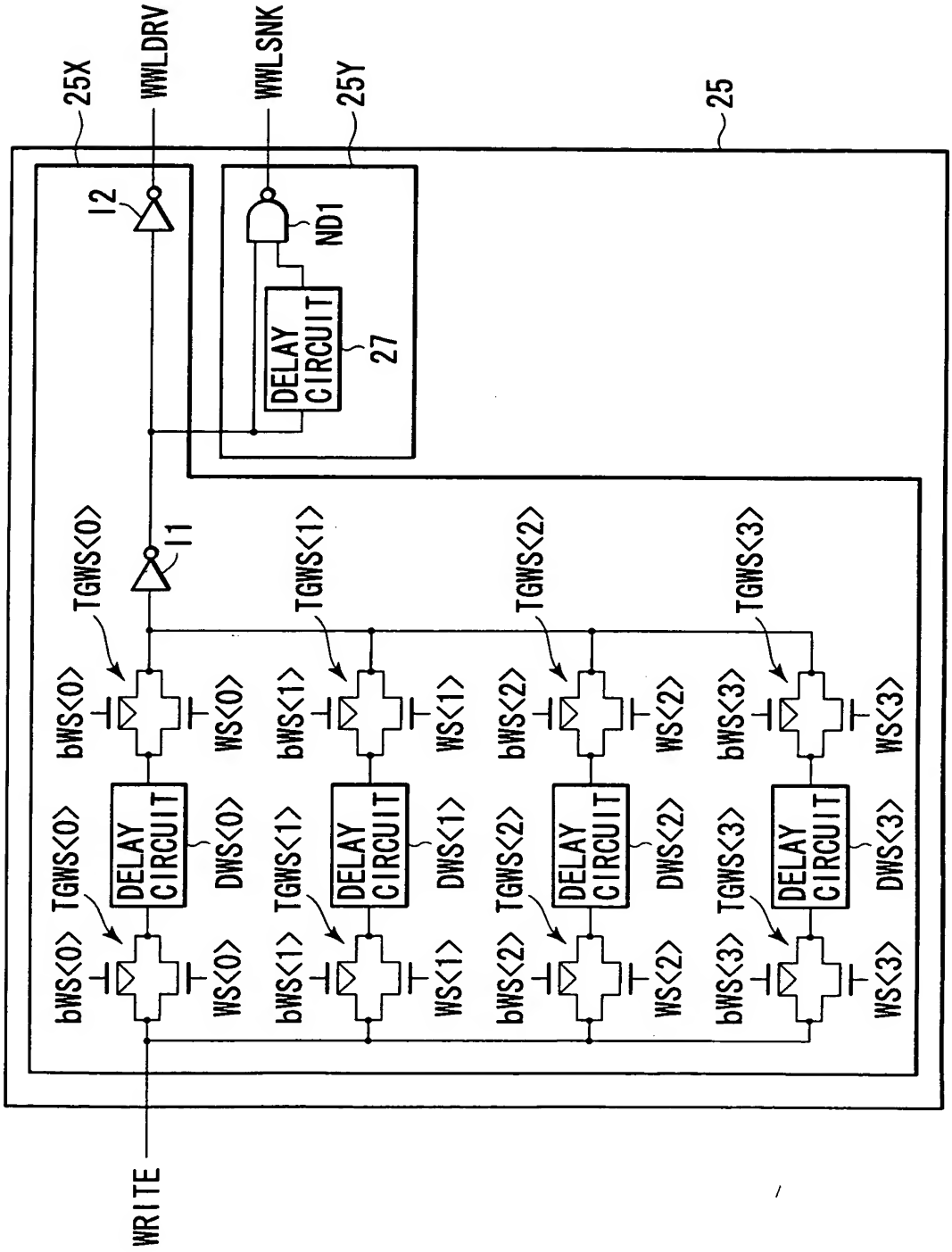

25X
WWLDRV
WWLSNK
25Y
25
I2
ND1
DELAY CIRCUIT
27
I1
TGWS<0>
TGWS<1>
TGWS<2>
TGWS<3>
bWS<0>
WS<0>
bWS<1>
WS<1>
bWS<2>
WS<2>
bWS<3>
WS<3>
DELAY CIRCUIT
DWS<0>
DWS<1>
DWS<2>
DWS<3>
WRITE

FIG. 39

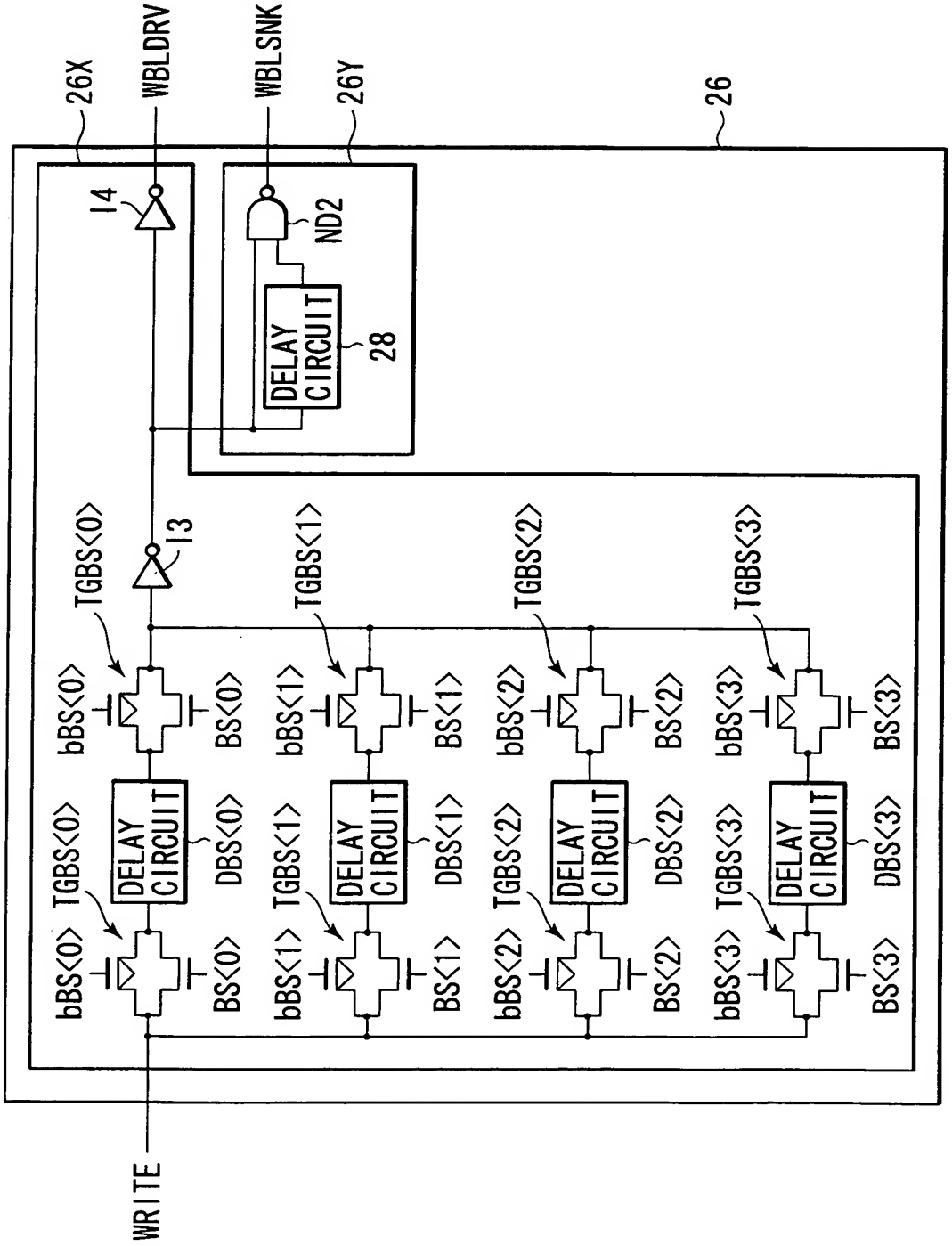

26X
WBLDRV
WBLSNK
26Y
26
14
ND2
DELAY CIRCUIT
28
13
TGBS<0>
TGBS<1>
TGBS<2>
TGBS<3>
bBS<0>
BS<0>
bBS<1>
BS<1>
bBS<2>
BS<2>
bBS<3>
BS<3>
DELAY CIRCUIT
DBS<0>
DBS<1>
DBS<2>
DBS<3>
WRITE

FIG. 40

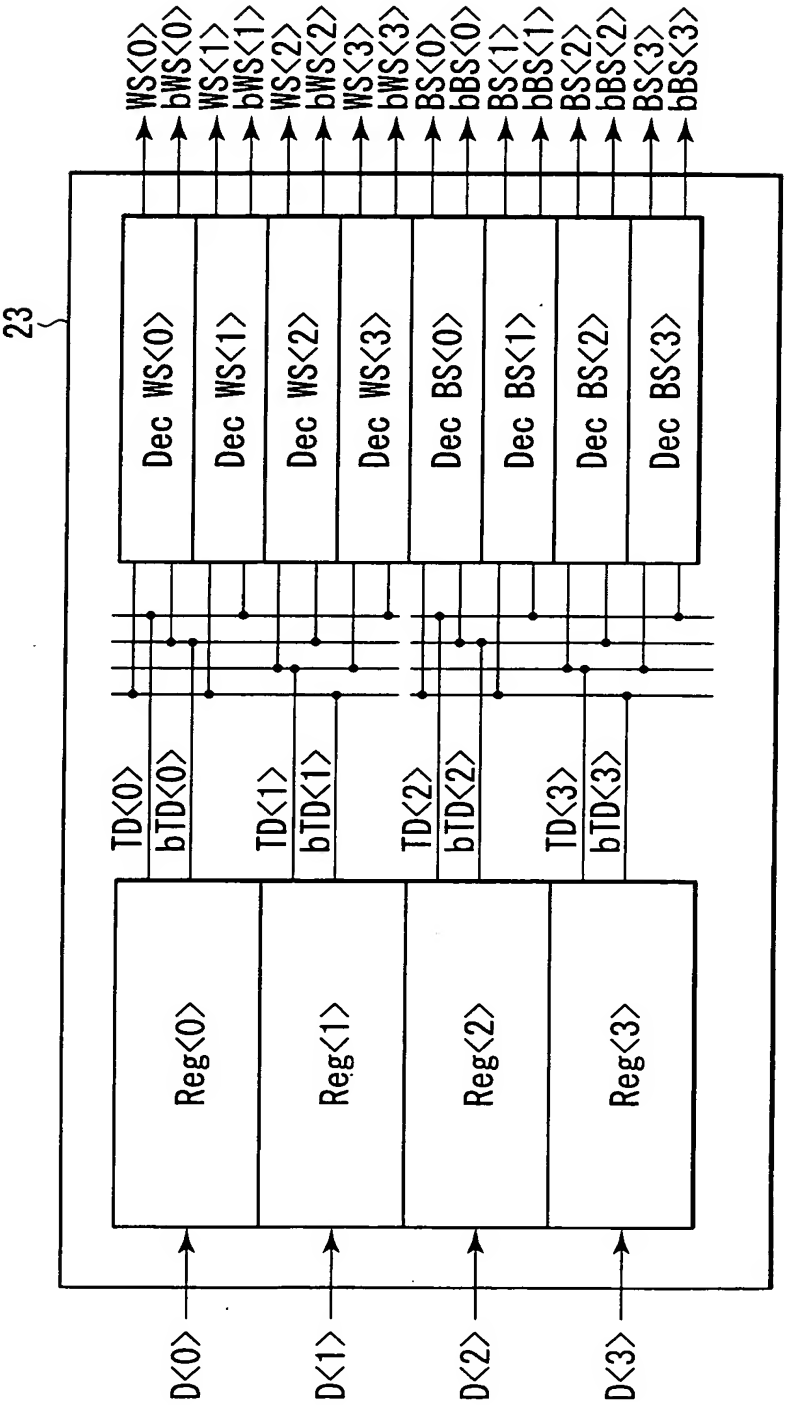

23
WS<0>
bWS<0>
WS<1>
bWS<1>
WS<2>
bWS<2>
WS<3>
bWS<3>
BS<0>
bBS<0>
BS<1>
bBS<1>
BS<2>
bBS<2>
BS<3>
bBS<3>
Dec WS<0>
Dec WS<1>
Dec WS<2>
Dec WS<3>
Dec BS<0>
Dec BS<1>
Dec BS<2>
Dec BS<3>
TD<0>
bTD<0>
TD<1>
bTD<1>
TD<2>
bTD<2>
TD<3>
bTD<3>
Reg<0>
Reg<1>
Reg<2>
Reg<3>
D<0>
D<1>
D<2>
D<3>

FIG. 41

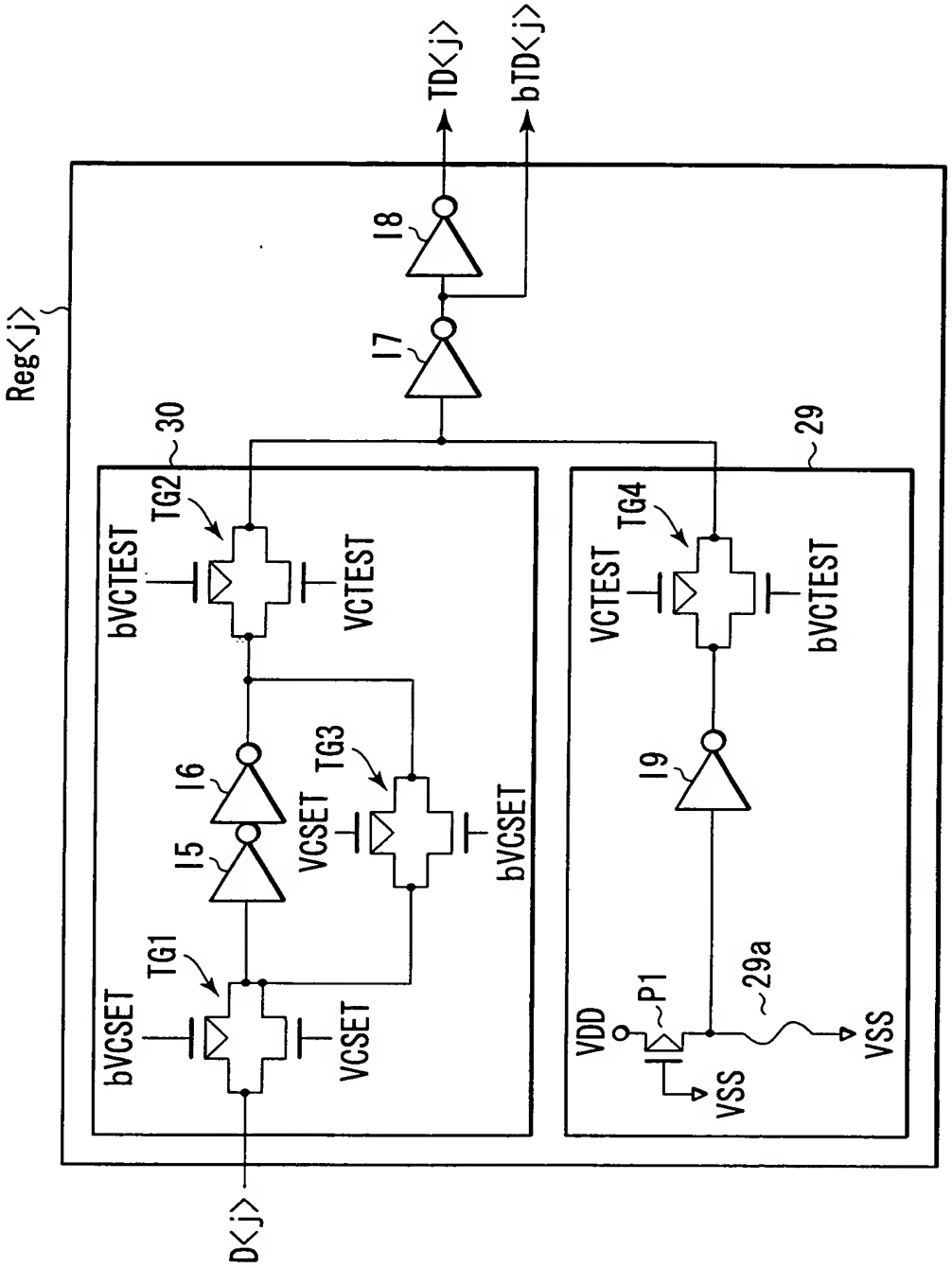

Reg<j>
TD<j>
bTD<j>
I8
I7
30
29
TG2
bVCTEST
VCTEST
TG4
VCTEST
bVCTEST
I6
I5
TG3
VCSET
bVCSET
I9
TG1
bVCSET
VCSET
VDD
P1
29a
VSS
VSS
VSS
D<j>

FIG. 42

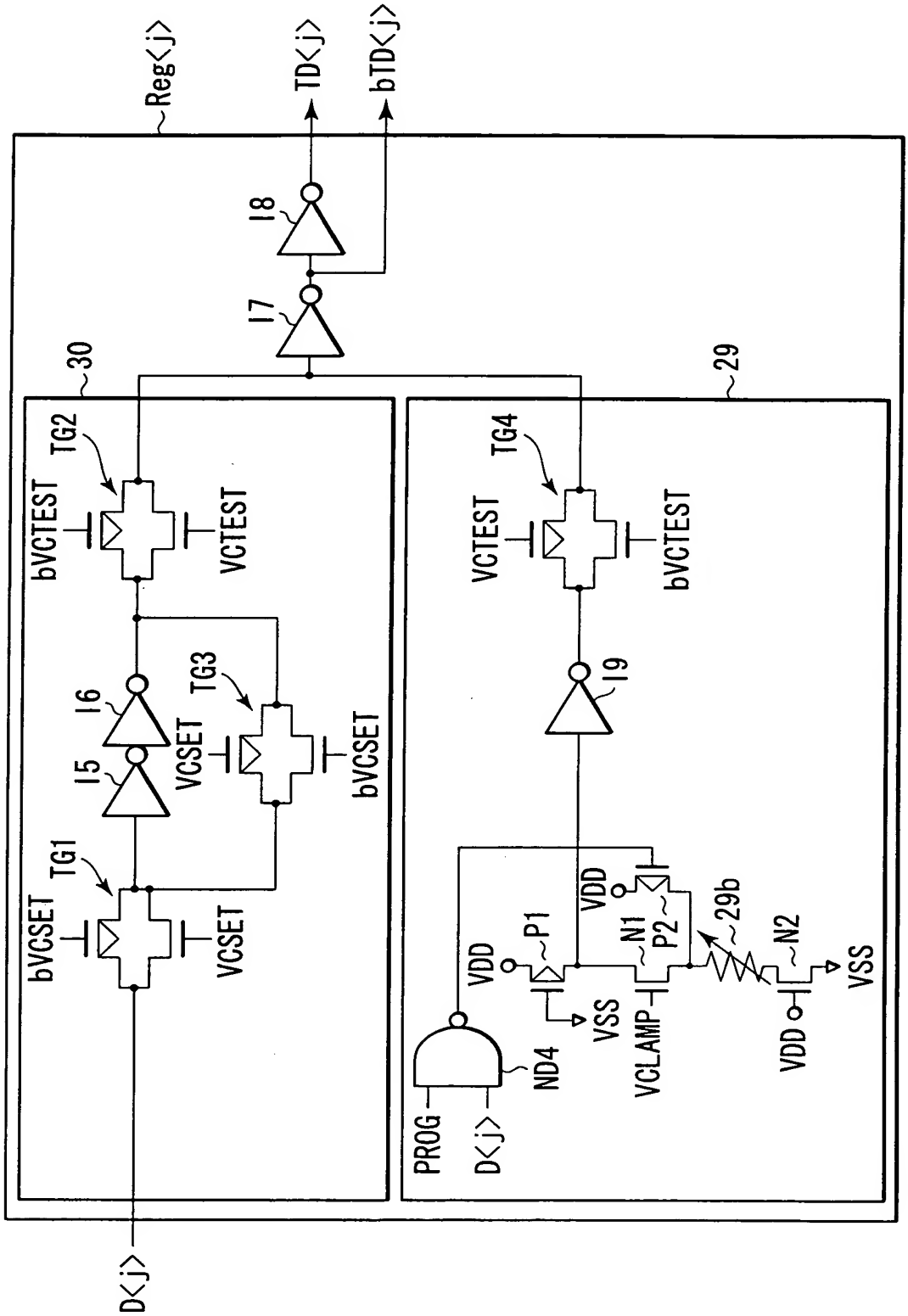

Reg<j>
TD<j>
bTD<j>
I8
I7
30
29
TG2
bVCTEST
VCTEST
TG4
VCTEST
bVCTEST
I6
I5
TG3
VCSET
bVCSET
I9
TG1
bVCSET
VCSET
VDD
P1
VDD
N1
P2
29b
N2
VSS
VSS
VCLAMP
VDD
ND4
PROG
D<j>
D<j>

FIG. 43

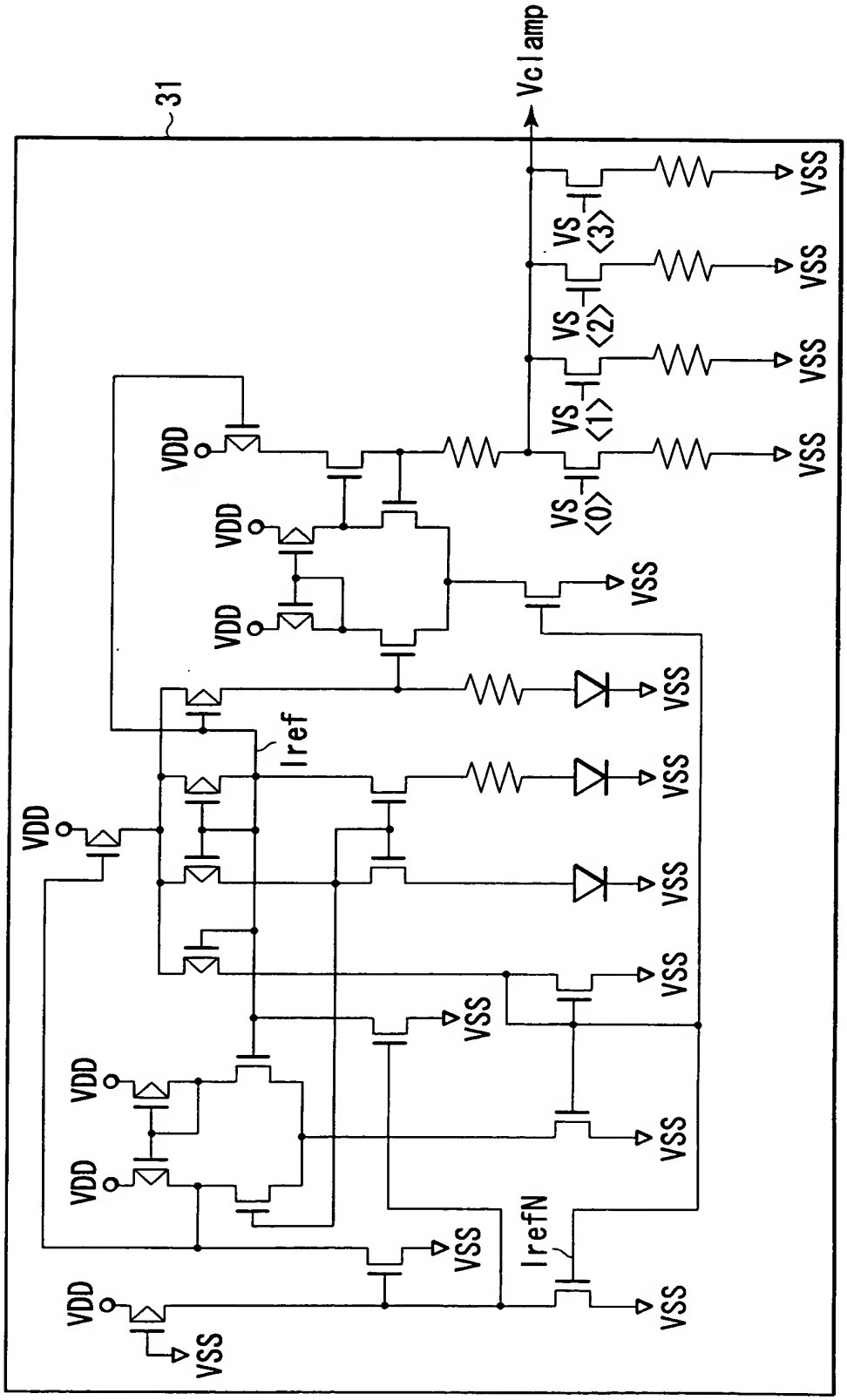


FIG. 44

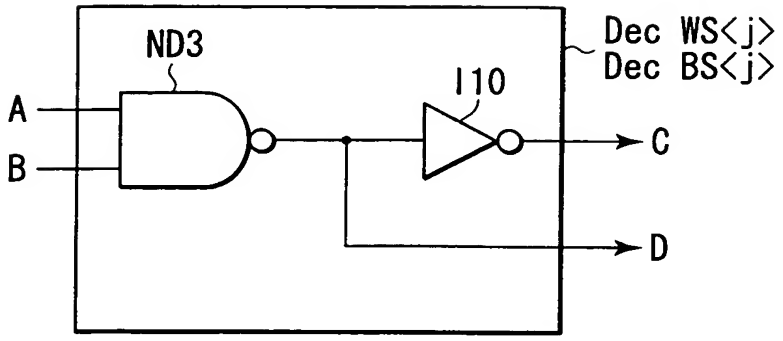


FIG. 45

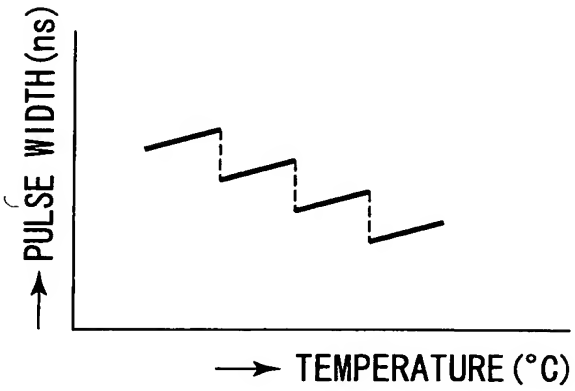


FIG. 46

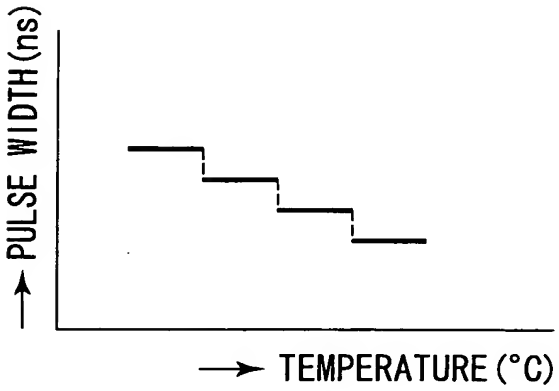


FIG. 47

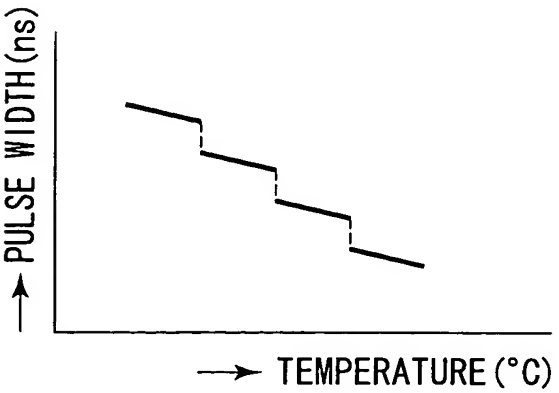


FIG. 48

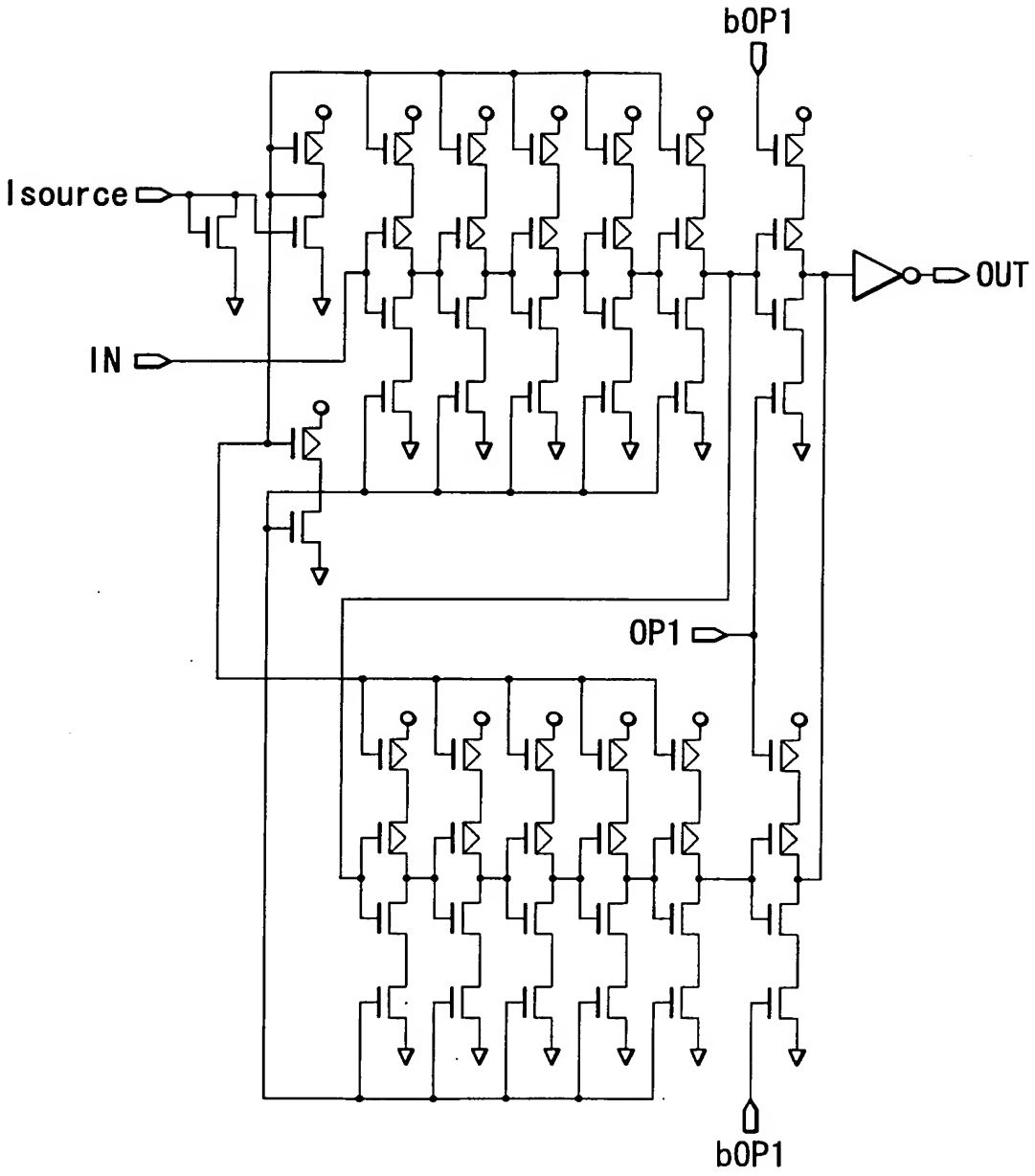


FIG. 49

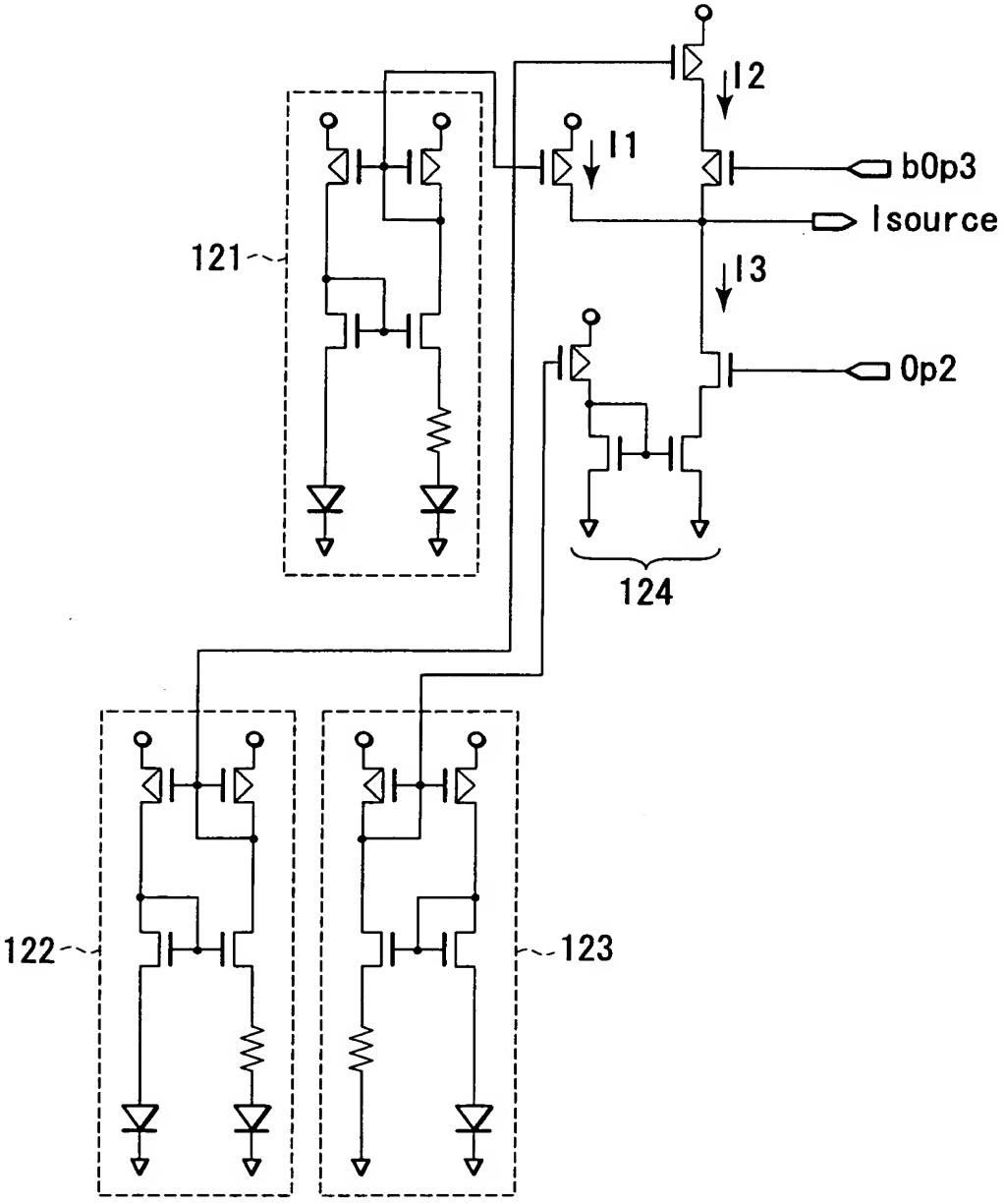


FIG. 50

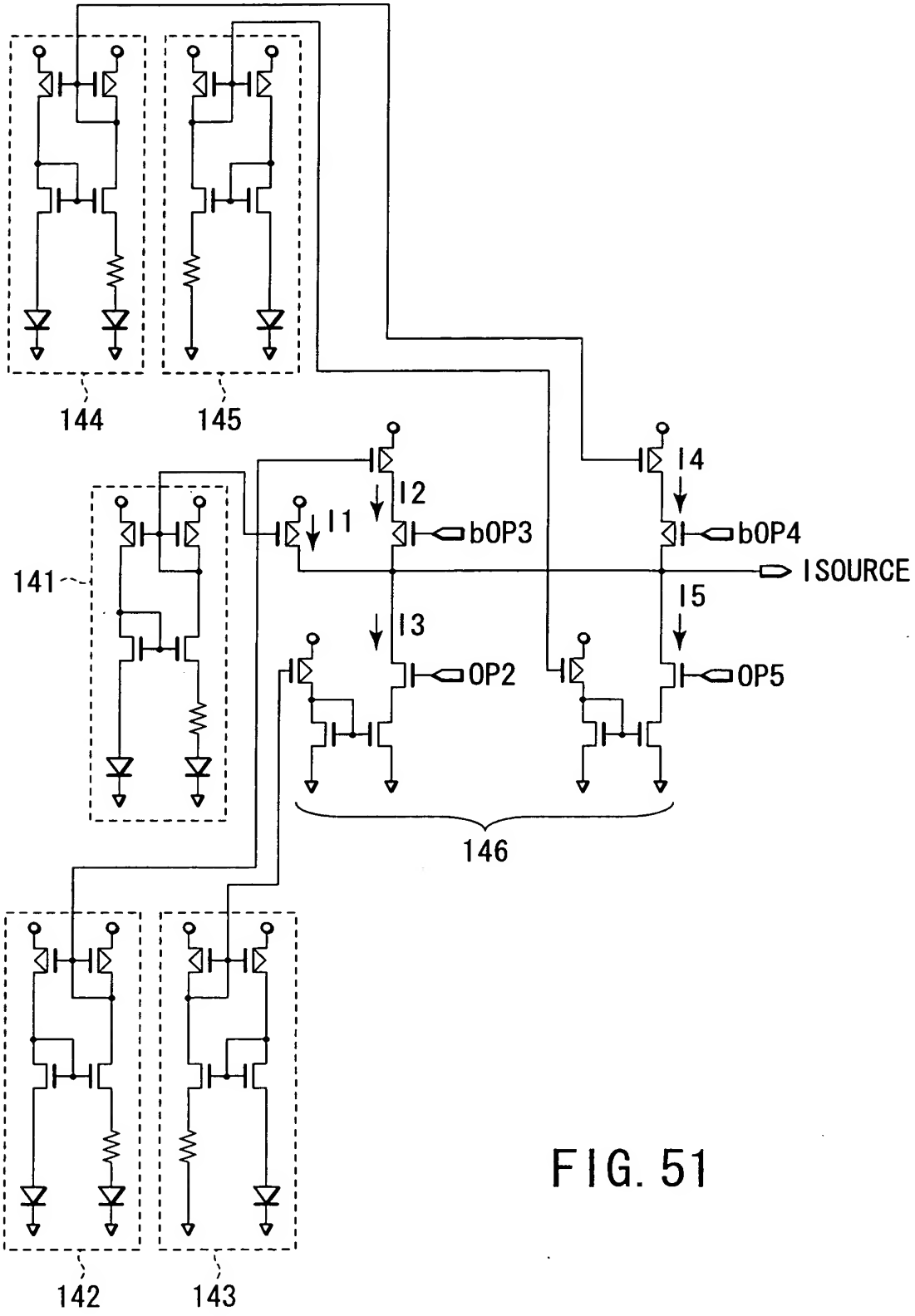


FIG. 51

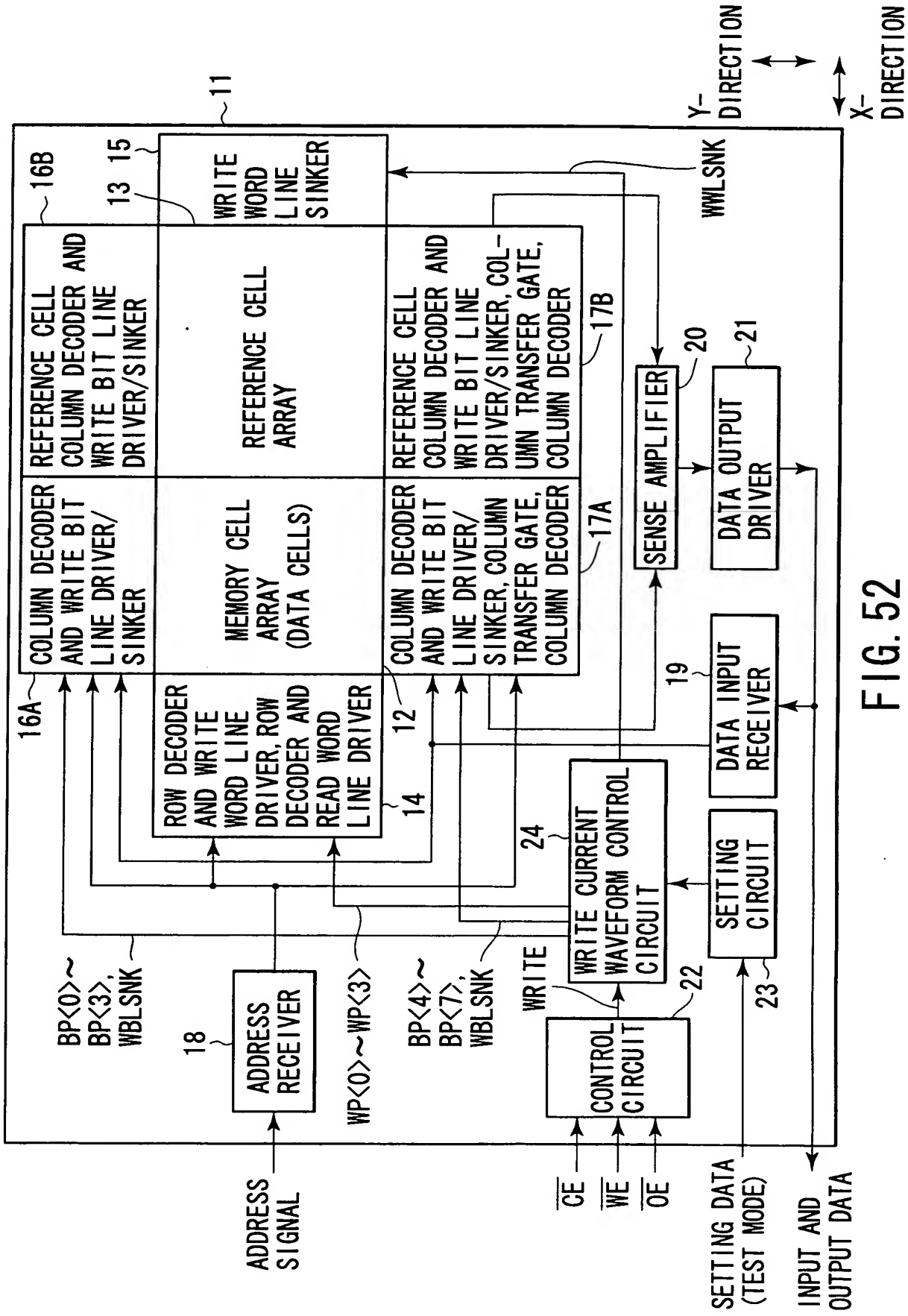

11
Y-DIRECTION
X-DIRECTION
16B
13
15
WRITE WORD LINE SINKER
WWLSNK
REFERENCE CELL COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER
REFERENCE CELL ARRAY
REFERENCE CELL COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER, COLUMN TRANSFER GATE, COLUMN DECODER
17B
20
21
SENSE AMPLIFIER
DATA OUTPUT DRIVER
16A
COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER
MEMORY CELL ARRAY (DATA CELLS)
COLUMN DECODER AND WRITE BIT LINE DRIVER/SINKER, COLUMN TRANSFER GATE, COLUMN DECODER
17A
ROW DECODER AND WRITE WORD LINE DRIVER, ROW DECODER AND READ WORD LINE DRIVER
14
12
19
DATA INPUT RECEIVER
24
WRITE CURRENT WAVEFORM CONTROL CIRCUIT
BP<0>~BP<3>, WBLSNK
18
ADDRESS RECEIVER
WP<0>~WP<3>
BP<4>~BP<7>, WBLSNK
WRITE
SETTING CIRCUIT
22
23
CONTROL CIRCUIT
ADDRESS SIGNAL
CE
WE
OE
SETTING DATA (TEST MODE)
INPUT AND OUTPUT DATA

FIG. 52

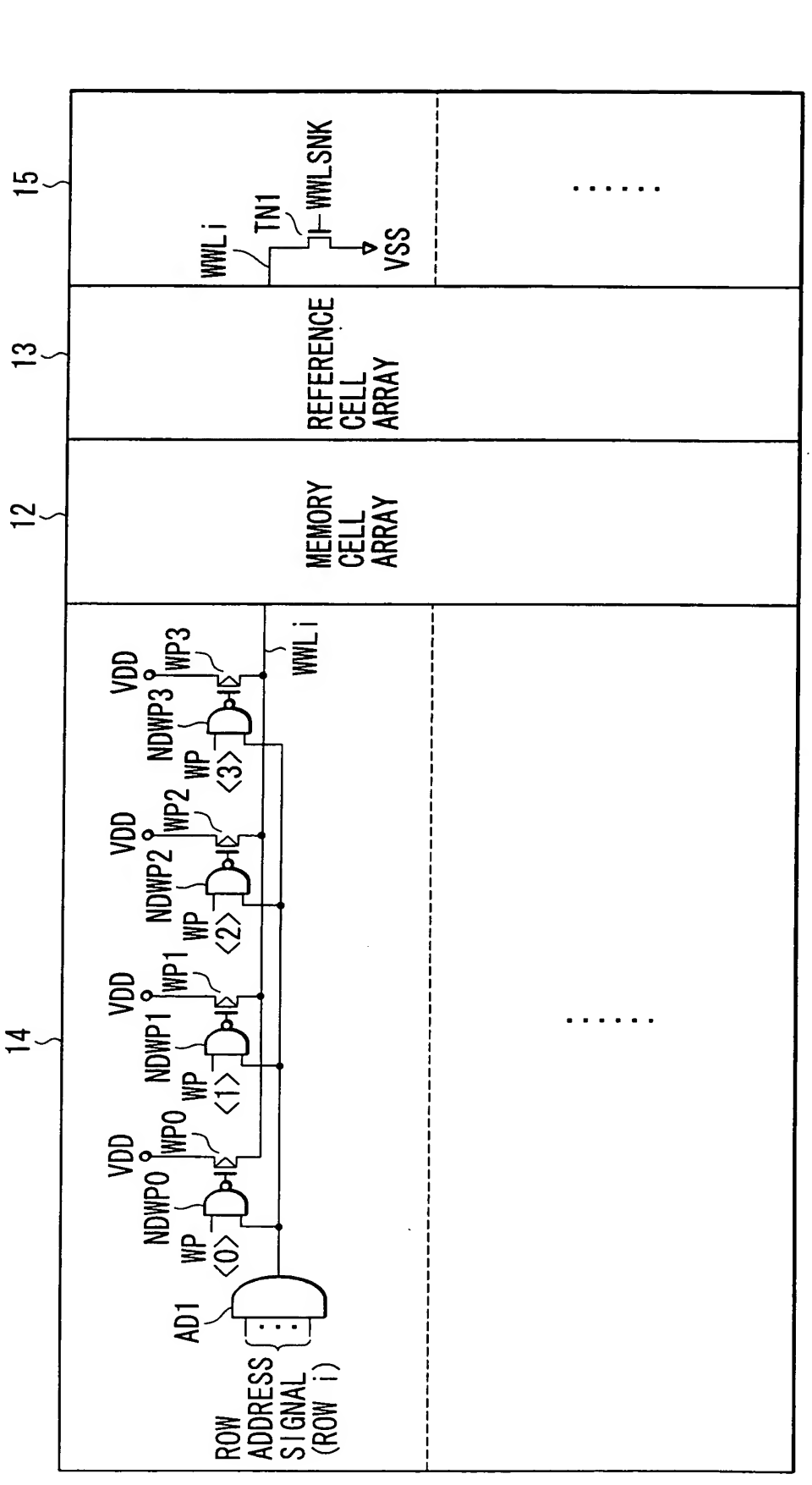

15
13
12
14
WWL i
TN1
WWLSNK
VSS
REFERENCE CELL ARRAY
MEMORY CELL ARRAY
Y-DIRECTION
X-DIRECTION
VDD
NDWP3
WP3
WP
<3>
NDWP2
WP2
<2>
NDWP1
WP1
<1>
NDWP0
WP0
<0>
AD1
ROW ADDRESS SIGNAL (ROW i)

FIG. 53

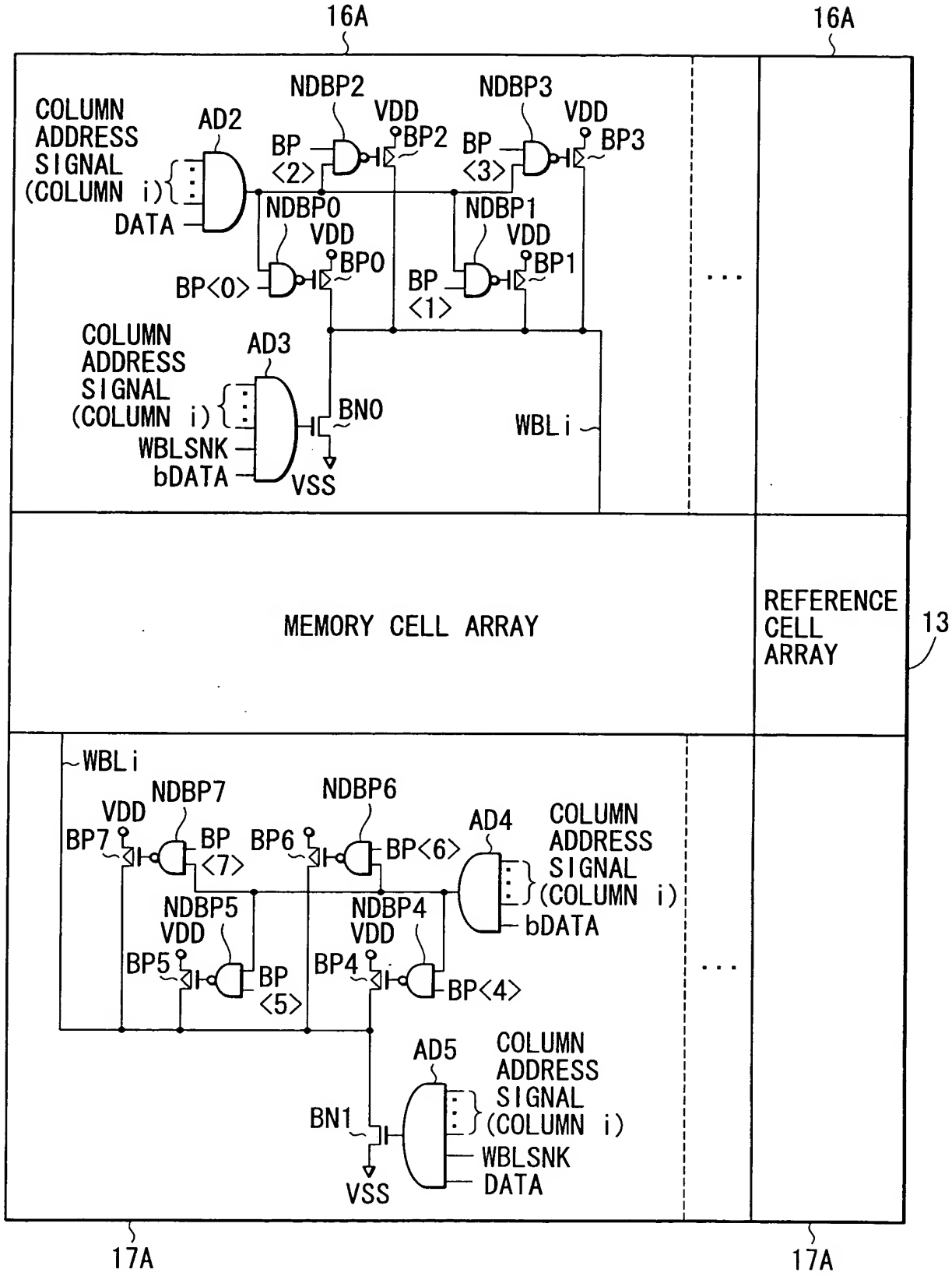

16A
16A
NDBP2
NDBP3
VDD
VDD
COLUMN ADDRESS SIGNAL (COLUMN i)
DATA
AD2
BP <2>
BP2
BP <3>
BP3
NDBP0
NDBP1
VDD
VDD
BP<0>
BP0
BP <1>
BP1
COLUMN ADDRESS SIGNAL (COLUMN i)
AD3
BN0
WBLSNK
bDATA
VSS
WBLi
MEMORY CELL ARRAY
REFERENCE CELL ARRAY
13
WBLi
NDBP7
NDBP6
VDD
BP7
BP <7>
BP6
BP<6>
AD4
COLUMN ADDRESS SIGNAL (COLUMN i)
bDATA
NDBP5
NDBP4
VDD
VDD
BP5
BP <5>
BP4
BP<4>
AD5
COLUMN ADDRESS SIGNAL (COLUMN i)
BN1
WBLSNK
DATA
VSS
17A
17A

FIG. 54

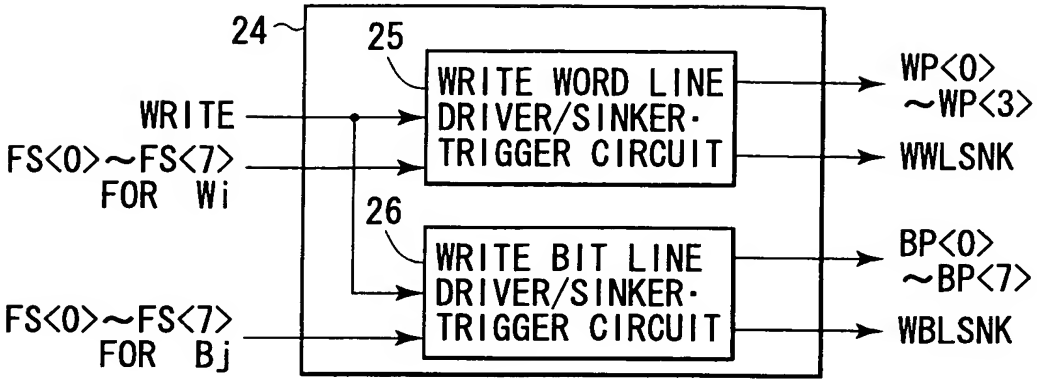

24
25
WRITE WORD LINE DRIVER/SINKER· TRIGGER CIRCUIT
WRITE
FS<0>~FS<7> FOR Wi
WP<0> ~WP<3>
WWLSNK
26
WRITE BIT LINE DRIVER/SINKER· TRIGGER CIRCUIT
FS<0>~FS<7> FOR Bj
BP<0> ~BP<7>
WBLSNK

FIG. 55

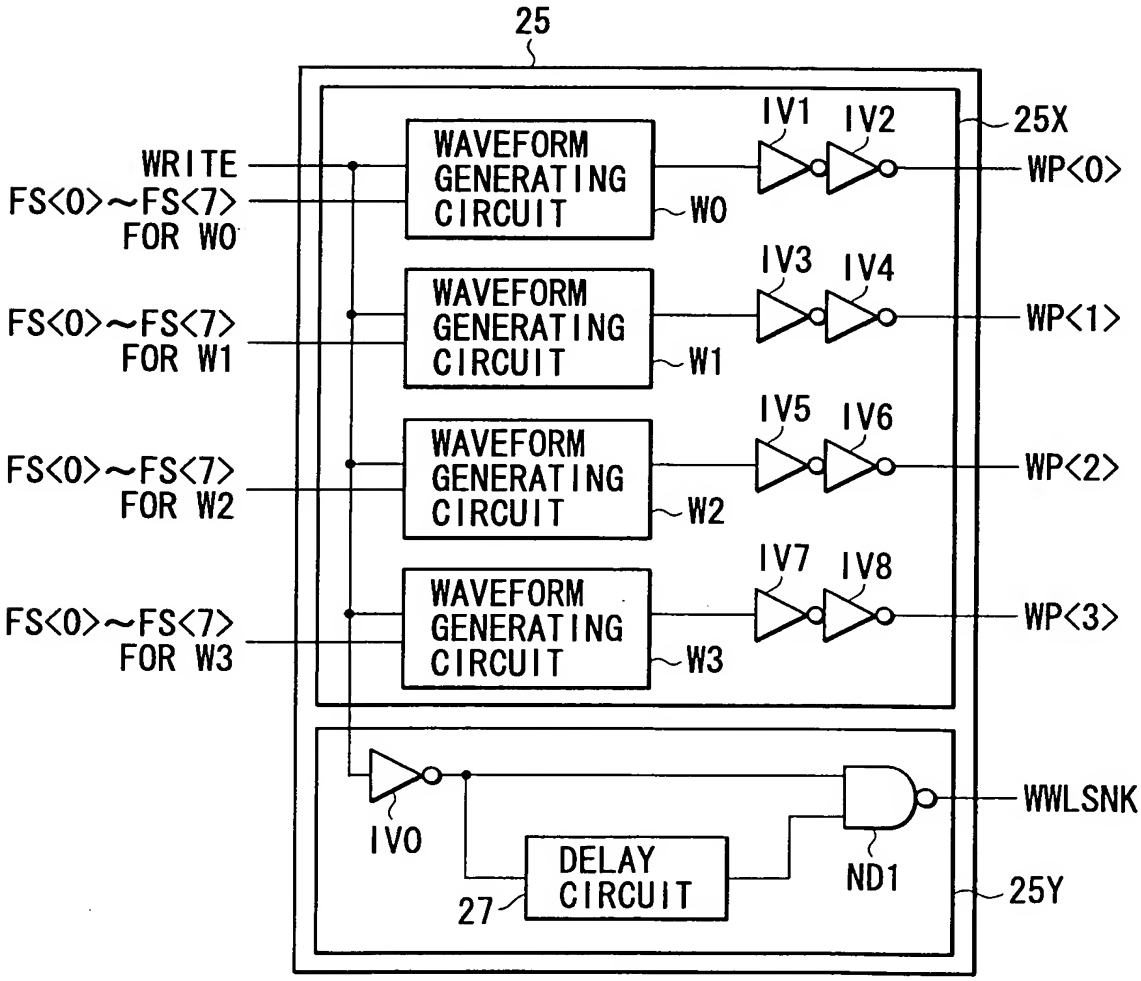

25
WAVEFORM GENERATING CIRCUIT
W0
W1
W2
W3
IV1
IV2
IV3
IV4
IV5
IV6
IV7
IV8
25X
WRITE
FS<0>~FS<7> FOR W0
FS<0>~FS<7> FOR W1
FS<0>~FS<7> FOR W2
FS<0>~FS<7> FOR W3
WP<0>
WP<1>
WP<2>
WP<3>
IV0
DELAY CIRCUIT
27
ND1
WWLSNK
25Y

FIG. 56

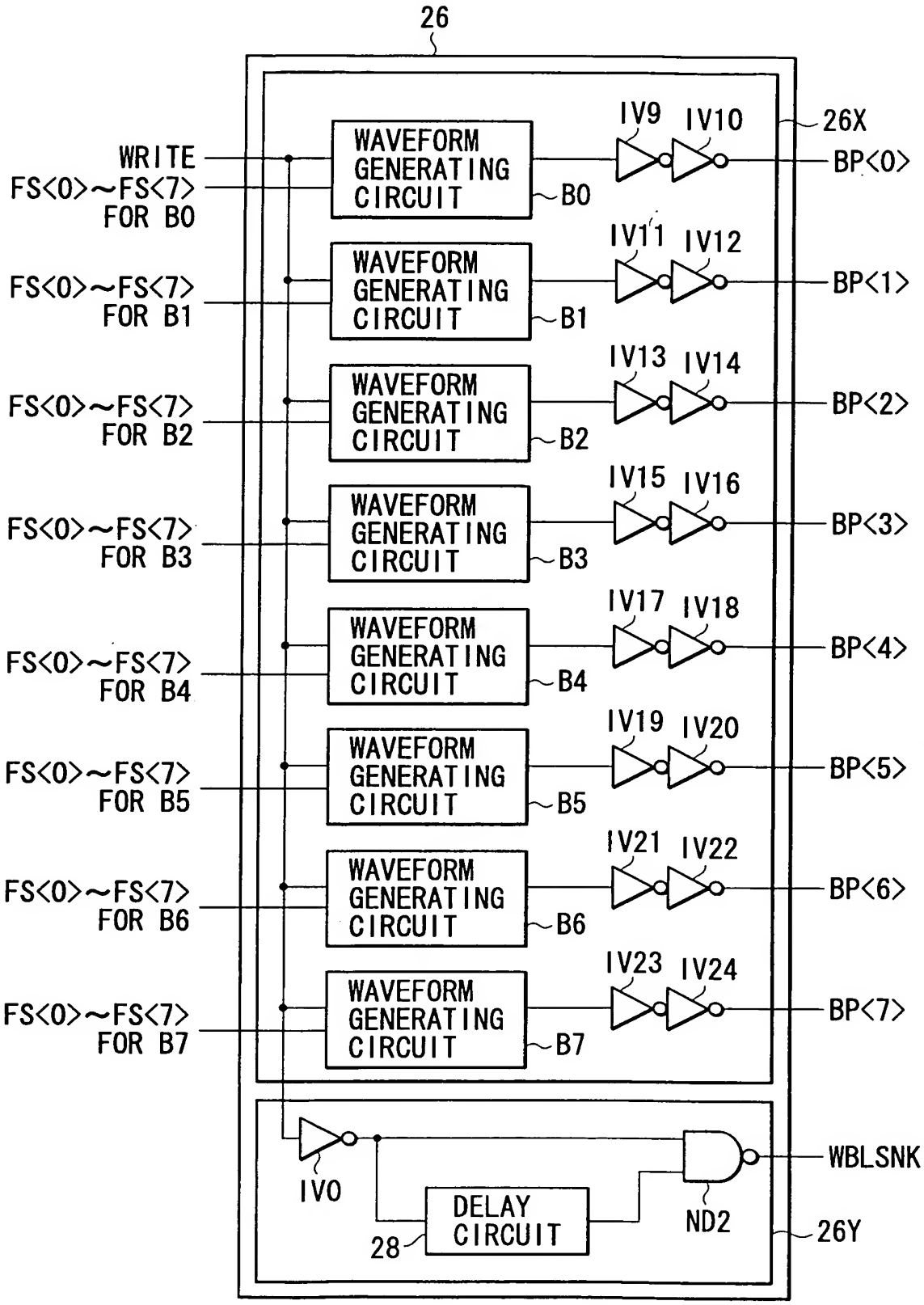

26
WRITE
FS<0>~FS<7>
FOR B0
FS<0>~FS<7>
FOR B1
FS<0>~FS<7>
FOR B2
FS<0>~FS<7>
FOR B3
FS<0>~FS<7>
FOR B4
FS<0>~FS<7>
FOR B5
FS<0>~FS<7>
FOR B6
FS<0>~FS<7>
FOR B7
WAVEFORM GENERATING CIRCUIT
B0
B1
B2
B3
B4
B5
B6
B7
IV9
IV10
IV11
IV12
IV13
IV14
IV15
IV16
IV17
IV18
IV19
IV20
IV21
IV22
IV23
IV24
26X
BP<0>
BP<1>
BP<2>
BP<3>
BP<4>
BP<5>
BP<6>
BP<7>
IV0
DELAY CIRCUIT
28
ND2
WBLSNK
26Y

FIG. 57

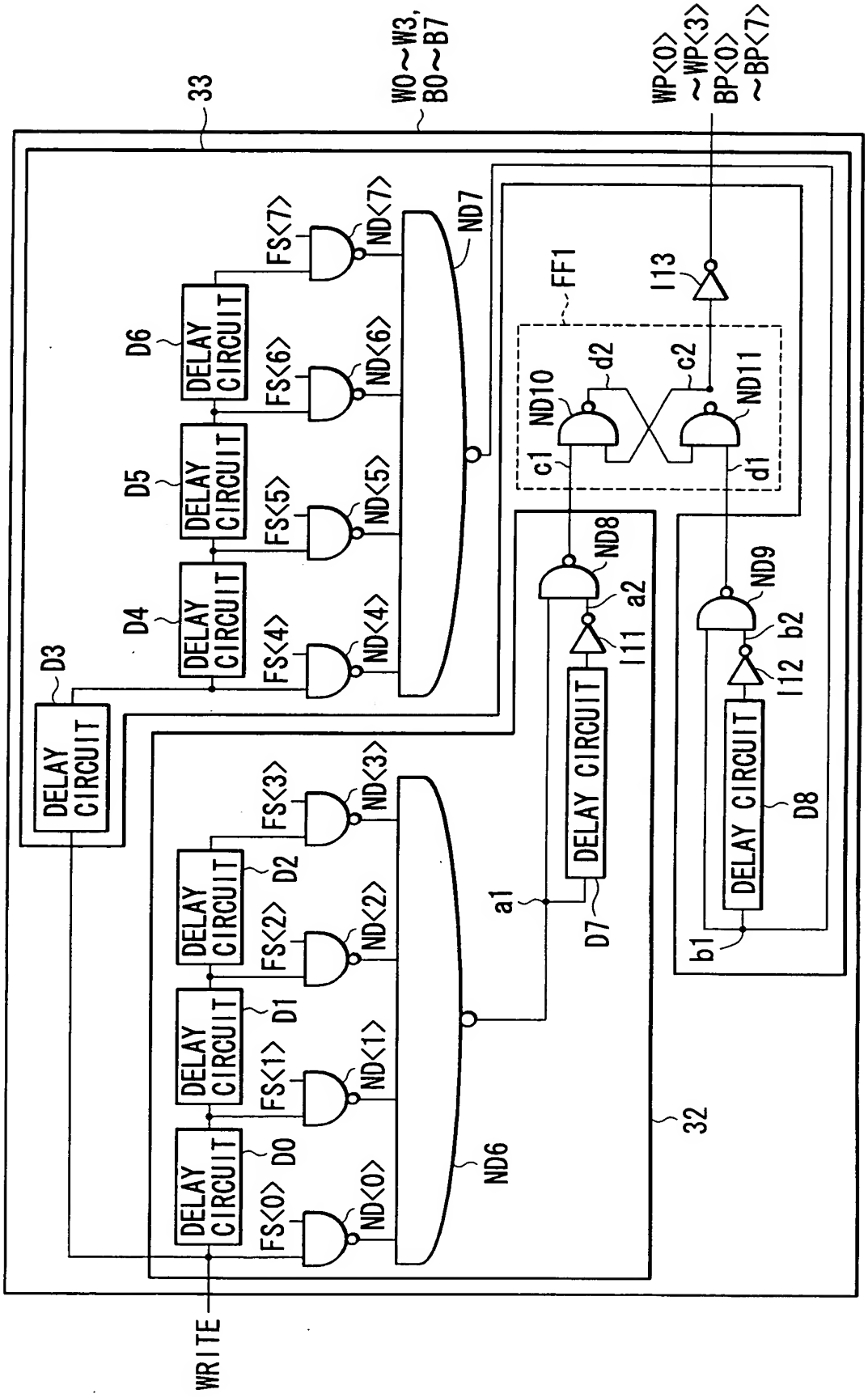

33
W0~W3,
B0~B7
WP<0>
~WP<3>
BP<0>
~BP<7>
WRITE
32
DELAY CIRCUIT
D0
D1
D2
D3
D4
D5
D6
D7
D8
FS<0>
FS<1>
FS<2>
FS<3>
FS<4>
FS<5>
FS<6>
FS<7>
ND<0>
ND<1>
ND<2>
ND<3>
ND<4>
ND<5>
ND<6>
ND<7>
ND6
ND7
ND8
ND9
ND10
ND11
FF1
I11
I12
I13
a1
a2
b1
b2
c1
c2
d1
d2

FIG. 58

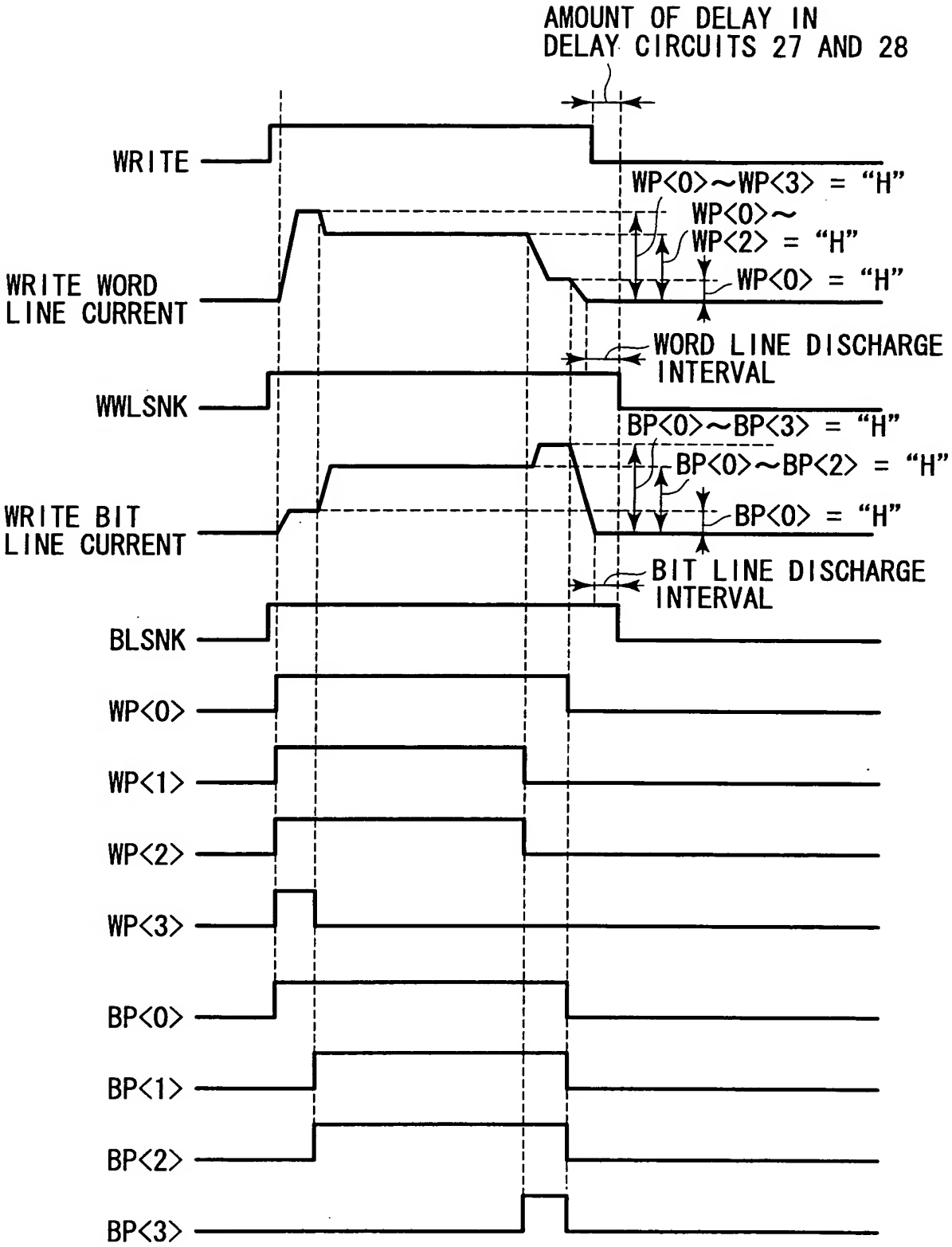

AMOUNT OF DELAY IN DELAY CIRCUITS 27 AND 28
WRITE
WP<0>~WP<3> = "H"
WP<0>~WP<2> = "H"
WP<0> = "H"
WRITE WORD LINE CURRENT
WORD LINE DISCHARGE INTERVAL
WWLSNK
BP<0>~BP<3> = "H"
BP<0>~BP<2> = "H"
BP<0> = "H"
WRITE BIT LINE CURRENT
BIT LINE DISCHARGE INTERVAL
BLSNK
WP<0>
WP<1>
WP<2>
WP<3>
BP<0>
BP<1>
BP<2>
BP<3>

FIG. 59

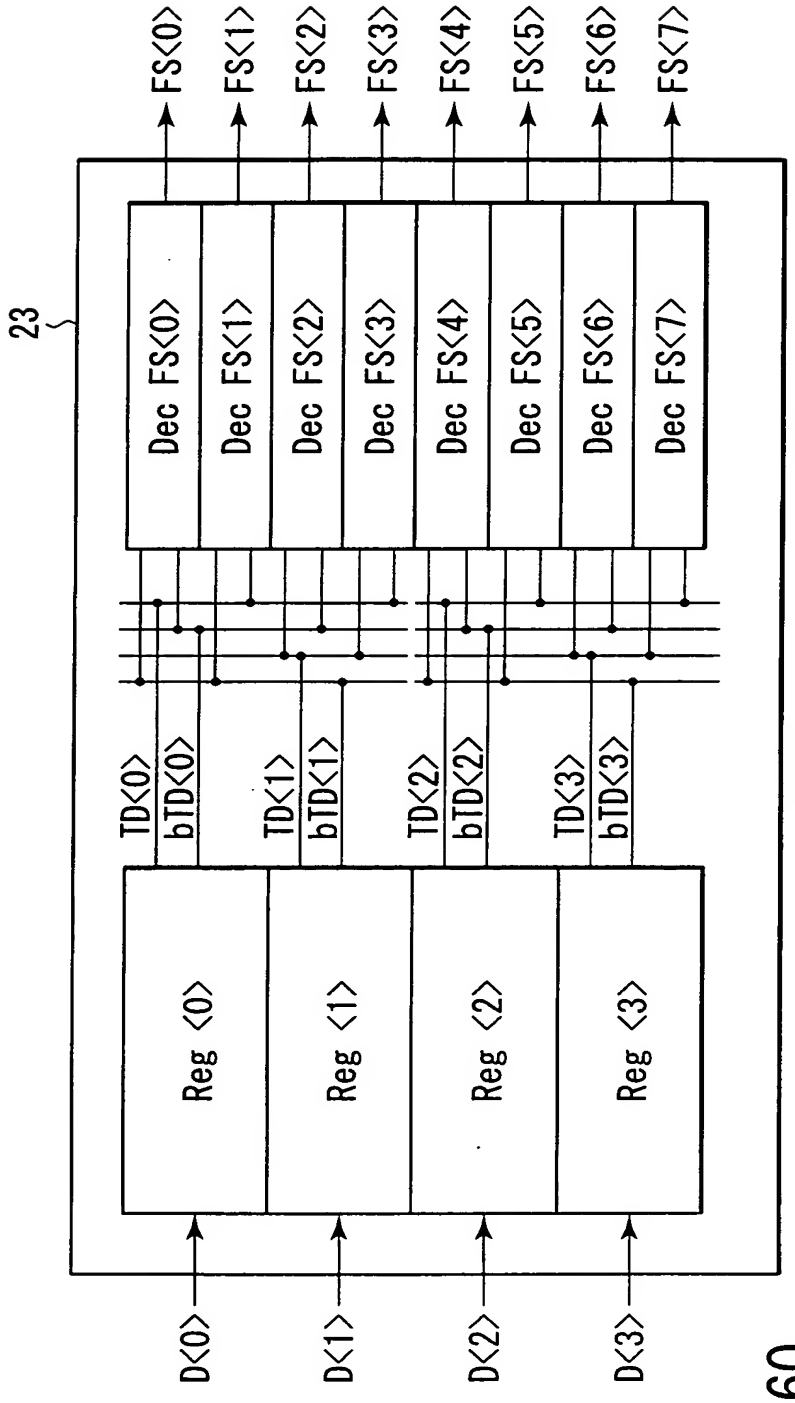

23
FS<0>
FS<1>
FS<2>
FS<3>
FS<4>
FS<5>
FS<6>
FS<7>
Dec FS<0>
Dec FS<1>
Dec FS<2>
Dec FS<3>
Dec FS<4>
Dec FS<5>
Dec FS<6>
Dec FS<7>
TD<0>
bTD<0>
TD<1>
bTD<1>
TD<2>
bTD<2>
TD<3>
bTD<3>
Reg <0>
Reg <1>
Reg <2>
Reg <3>
D<0>
D<1>
D<2>
D<3>

FIG. 60

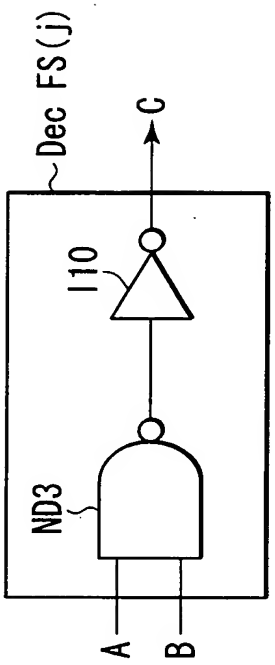

Dec FS(j)
C
I10
ND3
A
B

FIG. 61

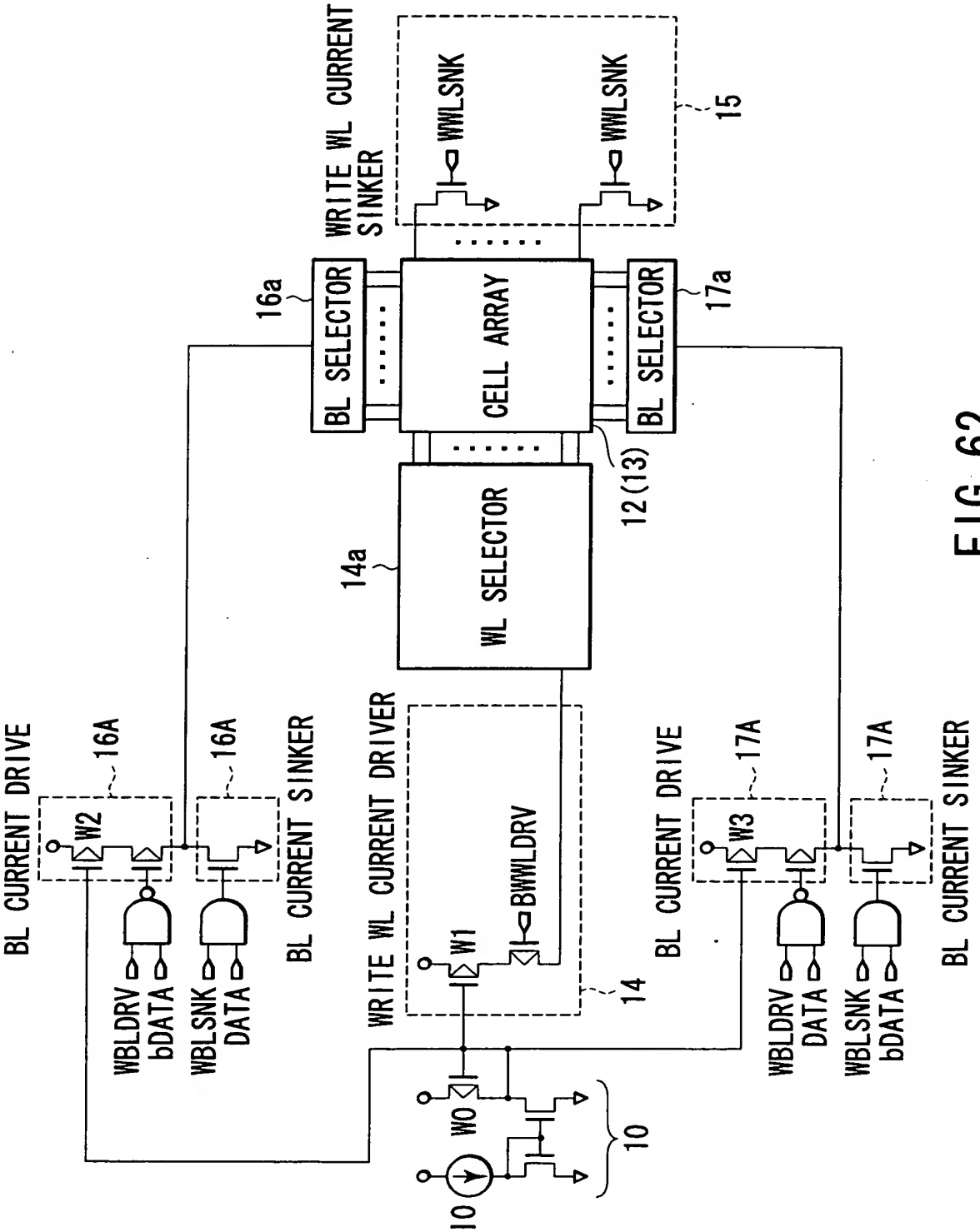

WRITE WL CURRENT SINKER
WWLSNK
WWLSNK
15
16a
BL SELECTOR
CELL ARRAY
BL SELECTOR
17a
12(13)
14a
WL SELECTOR
BL CURRENT DRIVE
16A
W2
WBLDRV
bDATA
WBLSNK
DATA
16A
BL CURRENT SINKER
WRITE WL CURRENT DRIVER
W1
BWWLDRV
14
BL CURRENT DRIVE
17A
W3
WBLDRV
DATA
WBLSNK
bDATA
17A
BL CURRENT SINKER
W0
10
10

FIG. 62

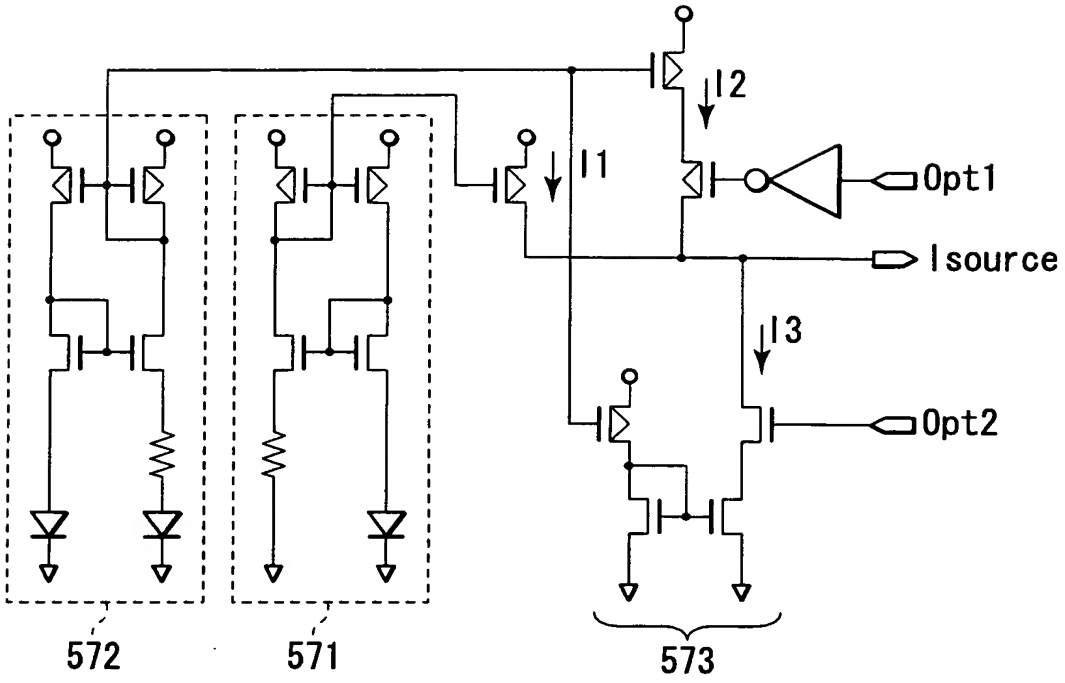

I2
I1
Opt1
Isource
I3
Opt2
572
571
573

FIG. 63

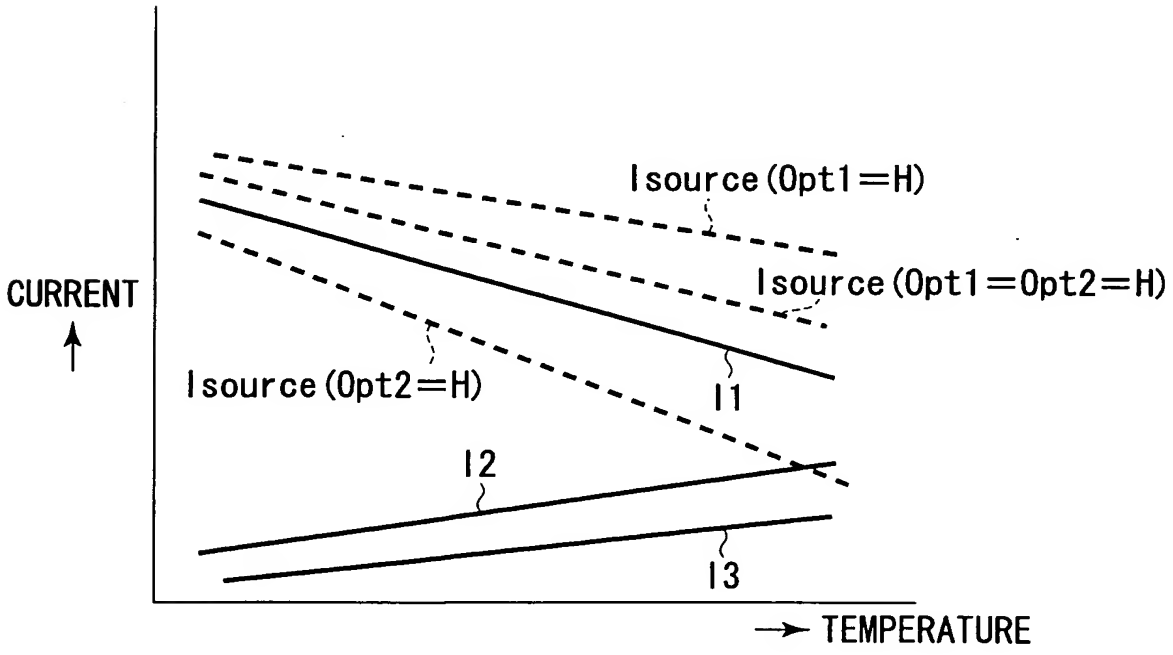

Isource (Opt1=H)
Isource (Opt1=Opt2=H)
CURRENT
Isource (Opt2=H)
I1
I2
I3
TEMPERATURE

FIG. 64

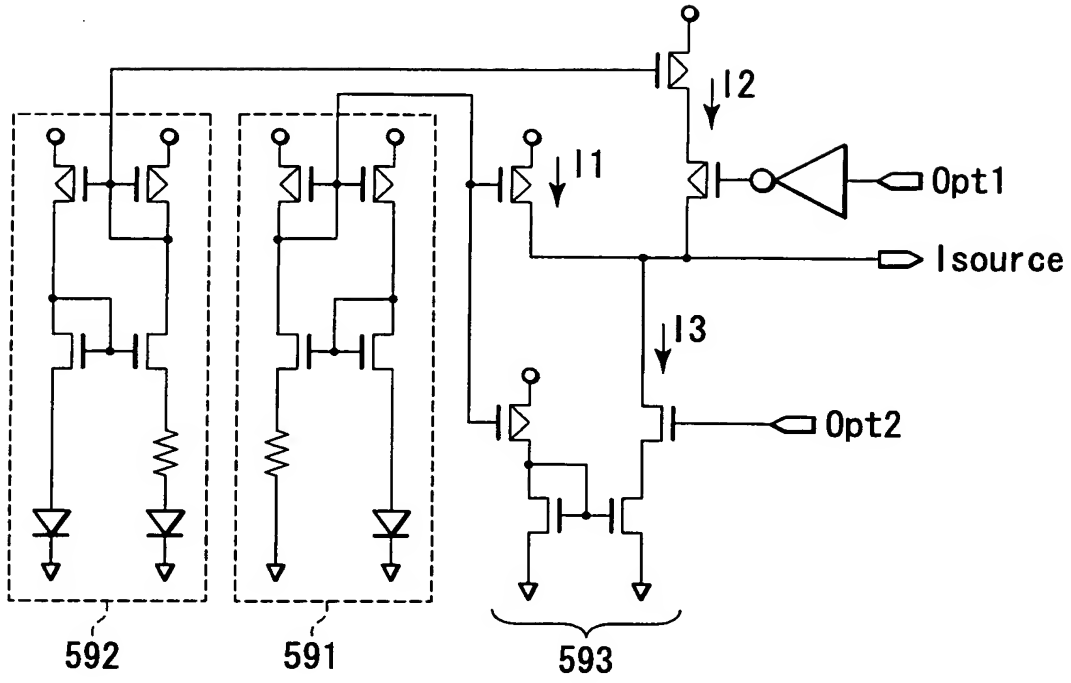

I2
I1
Opt1
Isource
I3
Opt2
592
591
593

FIG. 65

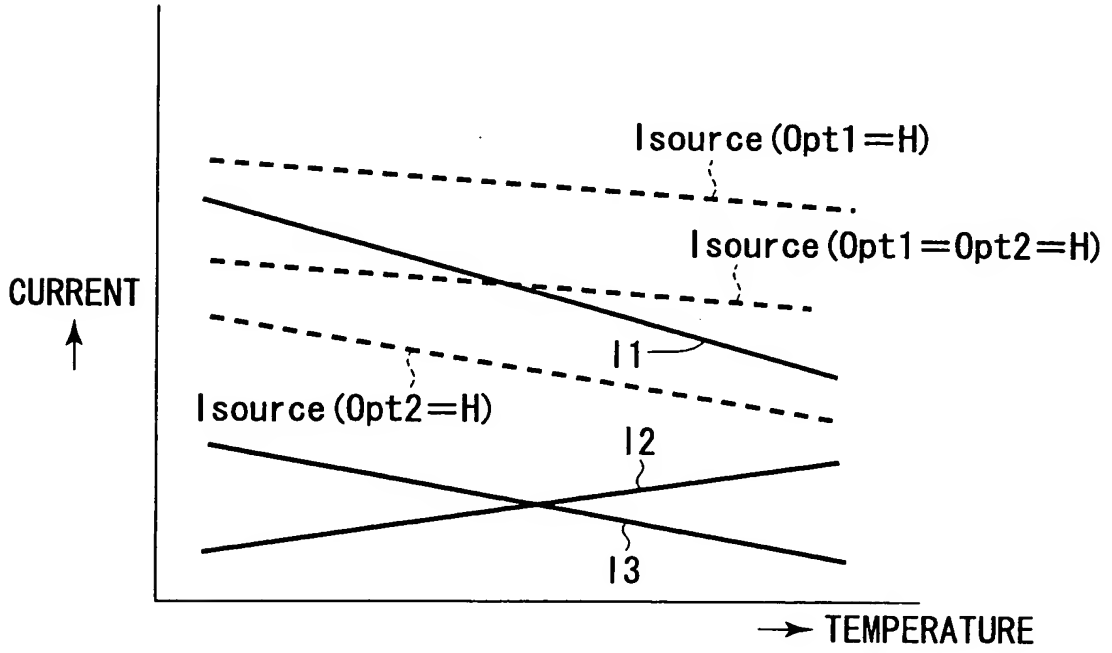

Isource (Opt1=H)
Isource (Opt1=Opt2=H)
CURRENT
I1
Isource (Opt2=H)
I2
I3
TEMPERATURE

FIG. 66

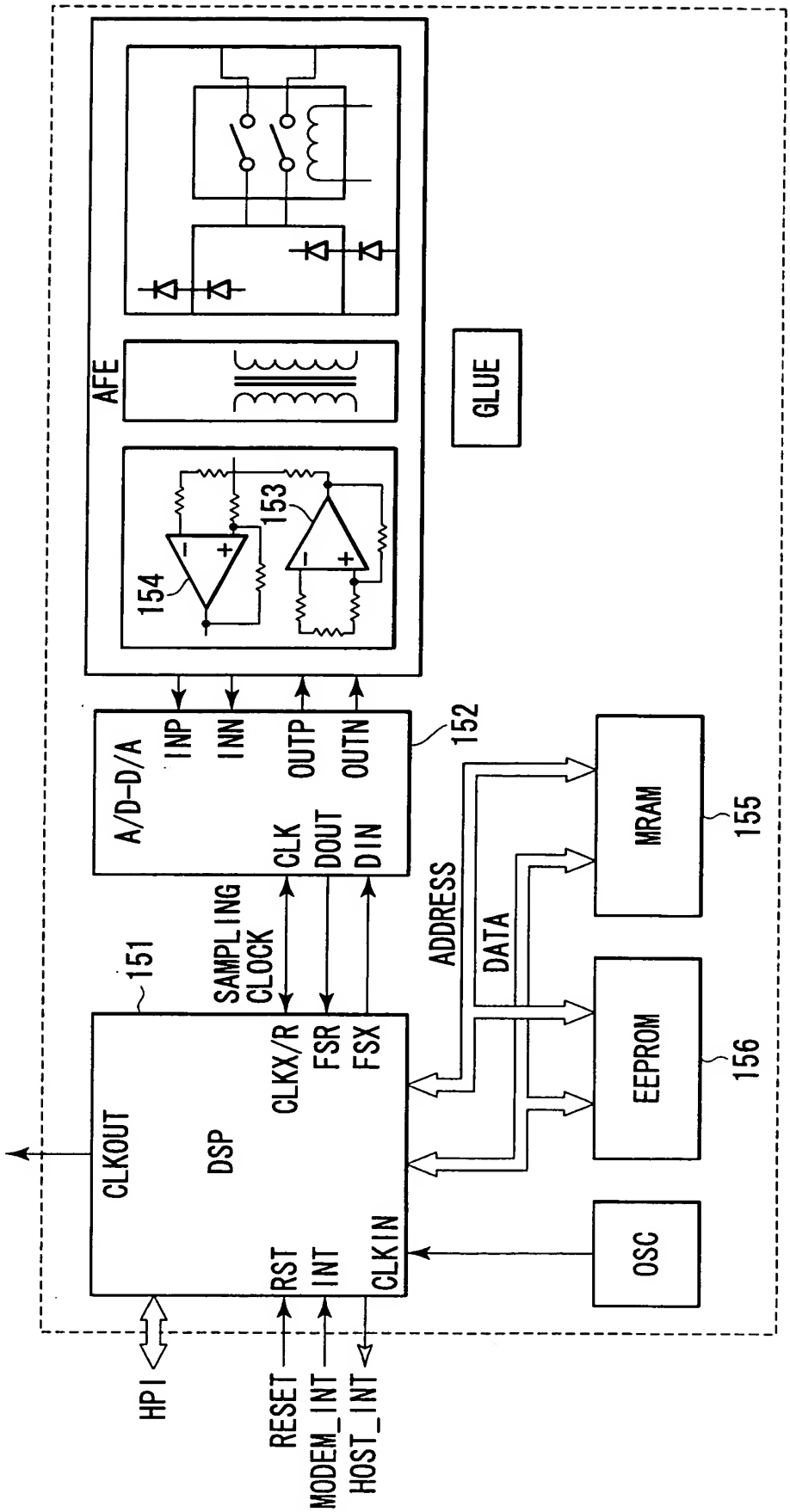

AFE
GLUE
154
153
A/D-D/A
INP
INN
OUTP
OUTN
CLK
DOUT
DIN
152
SAMPLING CLOCK
151
ADDRESS
DATA
MRAM
155
EEPROM
156
CLKOUT
DSP
CLKX/R
FSR
FSX
RST
INT
CLKIN
OSC
HPI
RESET
MODEM_INT
HOST_INT

FIG. 67

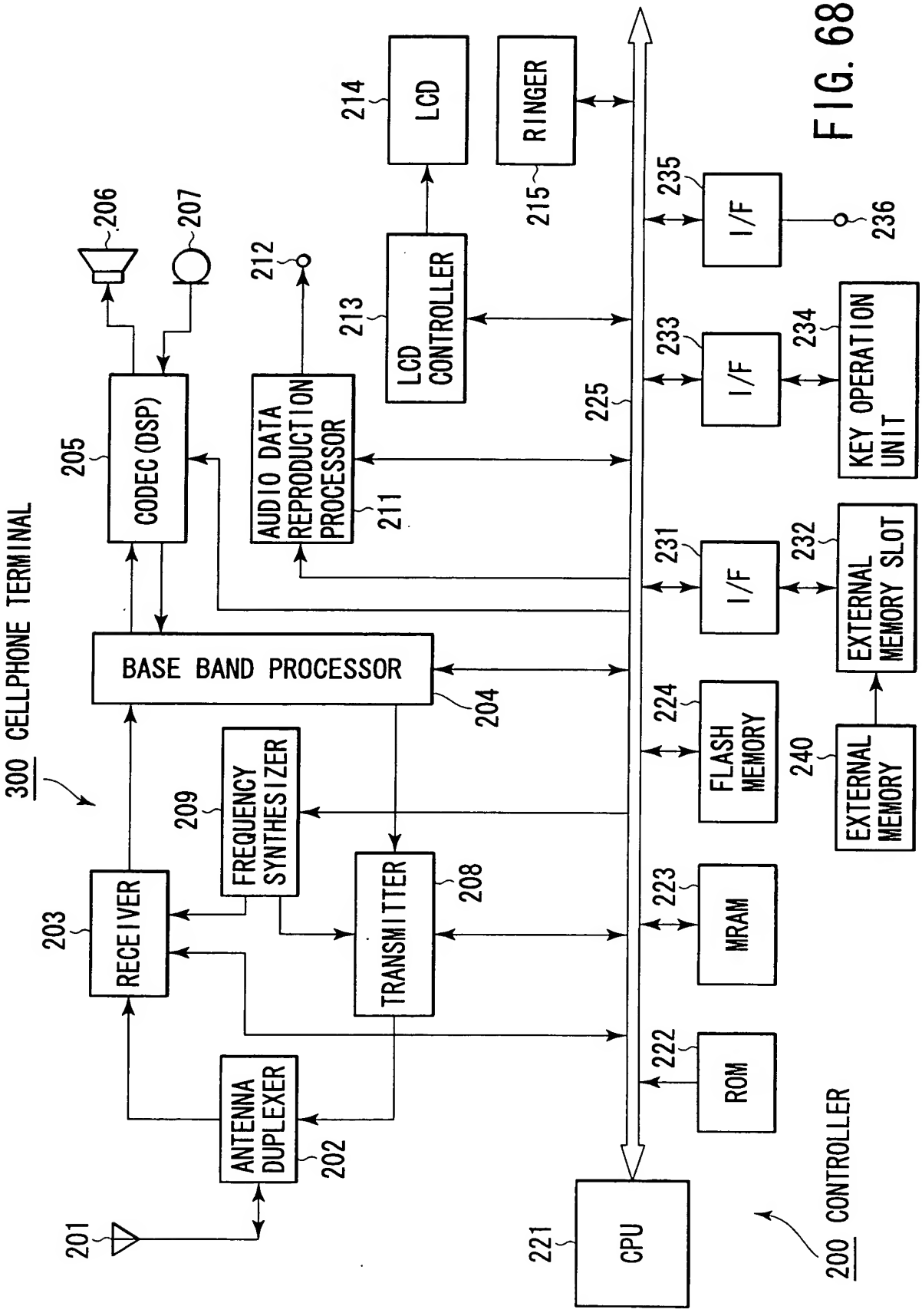

300 CELLPHONE TERMINAL
200 CONTROLLER
201
202
203
204
205
206
207
208
209
211
212
213
214
215
221
222
223
224
225
231
232
233
234
235
236
240
ANTENNA DUPLEXER
RECEIVER
TRANSMITTER
FREQUENCY SYNTHESIZER
BASE BAND PROCESSOR
CODEC (DSP)
AUDIO DATA REPRODUCTION PROCESSOR
LCD CONTROLLER
LCD
RINGER
I/F
I/F
I/F
KEY OPERATION UNIT
EXTERNAL MEMORY SLOT
EXTERNAL MEMORY
FLASH MEMORY
MRAM
ROM
CPU

FIG. 68

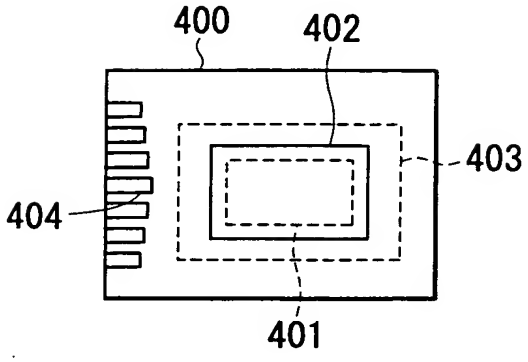


FIG. 69

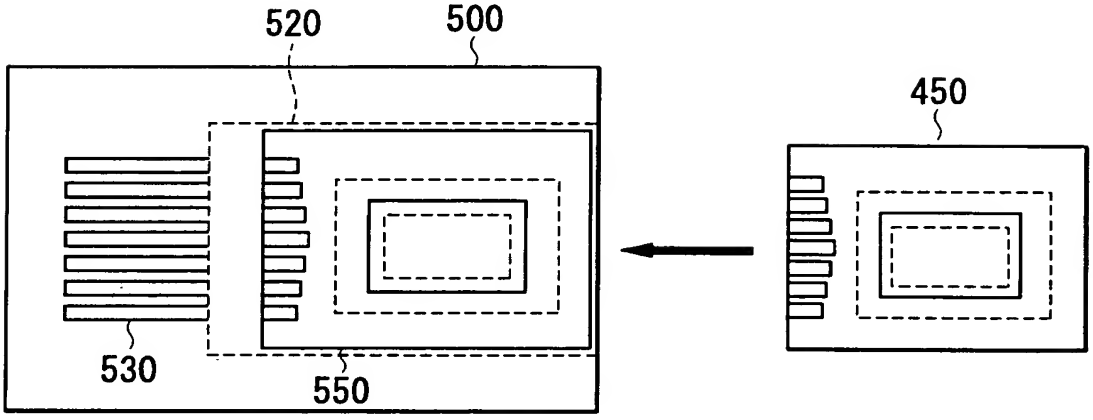
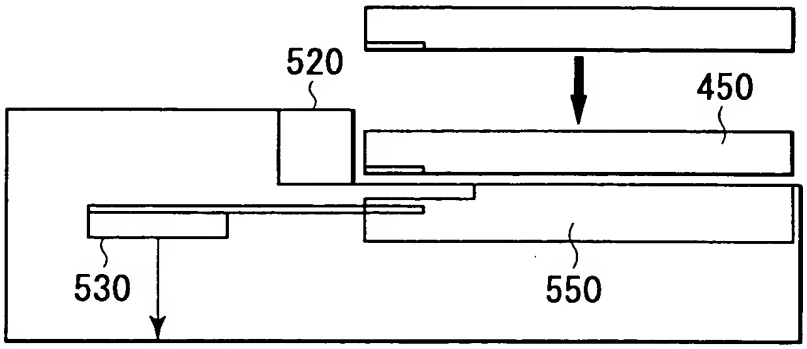


FIG. 70



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 72

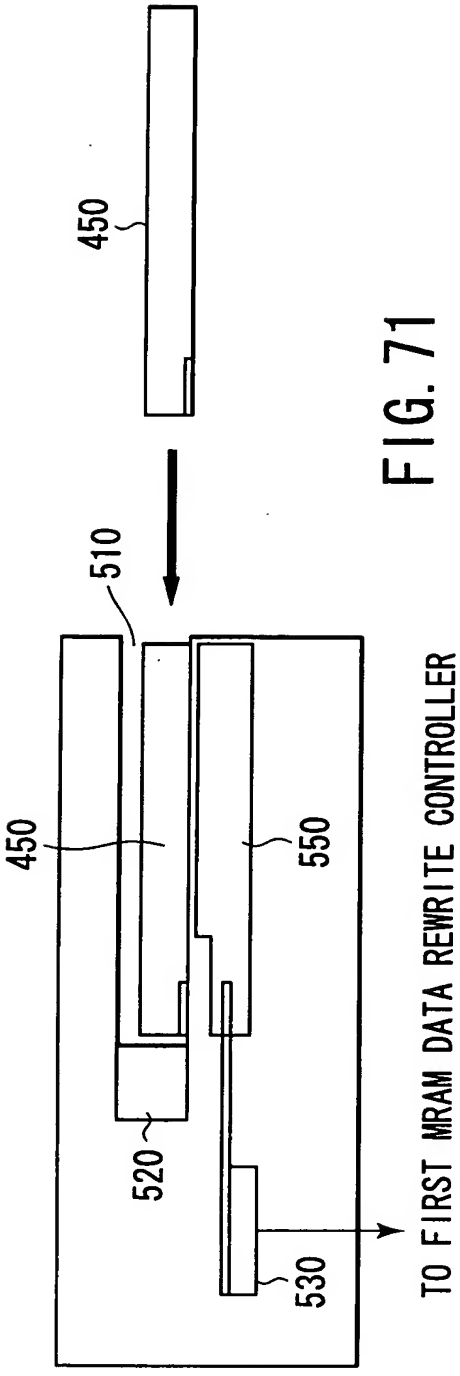

450
510
450
550
520
530
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 71

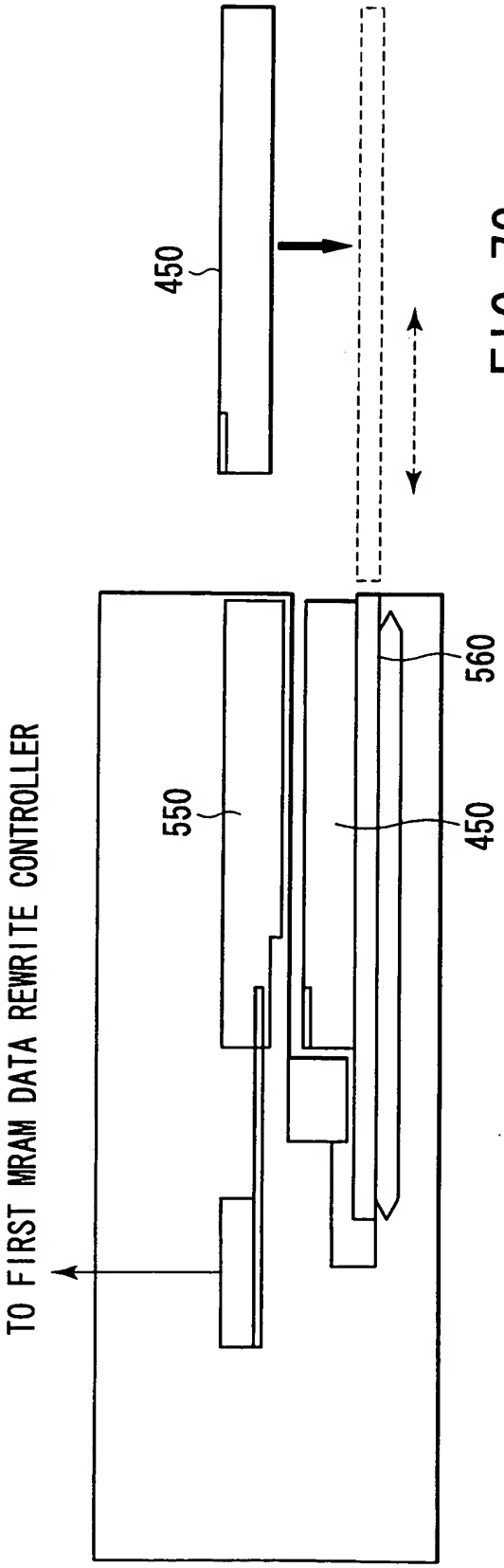

450
550
560
450
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 73